Nuclear Instruments and Methods in Physics Research A 623 (2010) 510–512

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

ATCA/μTCA for physics

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ARTICLE INFO

Available online 9 March 2010

Keywords:
ATCA
μTCA
Control system
Data acquisition system

ABSTRACT

ATCA/μTCA platforms are attractive because of the modern serial link architecture, high availability features and many packaging options. Less-demanding availability applications can be met economically by scaling back speed and redundancy. The ATCA specification was originally targeted for the Telecom industry but has gained recently a much wider user audience. The purpose of this paper is to report on present hardware and software R&D efforts where ATCA and μTCA are planned, already being used or in development using selected examples for accelerator and detectors in the Physics community. It will present also the status of a proposal for physics extensions to ATCA/μTCA specifications to promote inter-operability of laboratory and industry designs for physics.

1. Introduction

Engineers working in different laboratories starting new hardware developments discovered many limitations in factors used to date like VME. For new projects and experiments high availability, bandwidth, throughput and scalability, along with intelligent platform management are essential. Scalability implies modular design and flexibility in interconnections between modules, while availability requires redundancy and intelligent management for the platform hardware and software. Classical, parallel backplanes are not sufficient due to required data throughput and low latency. For large data acquisition and control systems (e.g. control systems for the European XFEL or planned like the International Linear Collider (ILC)) maintainability is crucial.

In VME based systems, fast and low-latency communication is realized via point-to-point connections between boards on front of the crate. In addition, input signals from accelerator cavities or detectors sensors as well as timing signals are most of the time connected directly to front panels. Quite often a few tens of cables are connected to a single board, making the maintenance very difficult and might cause damage to the cables or mistakes in connection during replacement of the boards.

A more complete description and details of the problems on the classical systems and new development based on the new standards can be found in Ref. [1].

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0168-9002/$ - see front matter © 2010 Published by Elsevier B.V.
doi:10.1016/j.nima.2010.03.053

2. ATCA/μTCA

The specification of the Advanced Telecom Computing Architecture (ATCA) and μTCA (also written as MTCA or microTCA) are described in PICMG 3.0 document [2]. This is the largest specifications effort made in the history of the PCI Industrial Computer Manufacturers Group (PICMG). With over 200 companies participating, including Sun, Intel, and Motorola, among many others, ATCA/μTCA are gaining wide acceptance as the new industry standard. xTCA specifies connectors, mechanics, power distribution, blade dimensions, and system management that are robust and independent of the switch fabric link technology used.

Key features of ATCA and μTCA are :

- A high throughput capacity (up to 2.5 Terabits).
- A highly scalable, switched fabric architecture, based on Gigabit Ethernet, InfiniBand or PCIExpress, overcomes the IO bottlenecks created by conventional bus-based architectures.
- Support for up to 200 W per board (blade) and as many as 14 boards per crate (shelf).
- Two power modules and power rails to each slot provide hardware redundancy, reducing single points of failure.
- Shelf availability up to 99.999 percent – only 5 min downtime per year.

The common module for both systems, ATCA and μTCA, is an Advanced Mezzanine Module (AMC), specified also by PICMG. The same module can be used in the small μTCA system as well as ATCA system, with the same functionality (HW and SW).

The main difference between ATCA and μTCA system, besides size, is the organization of the data transport in the crate. The

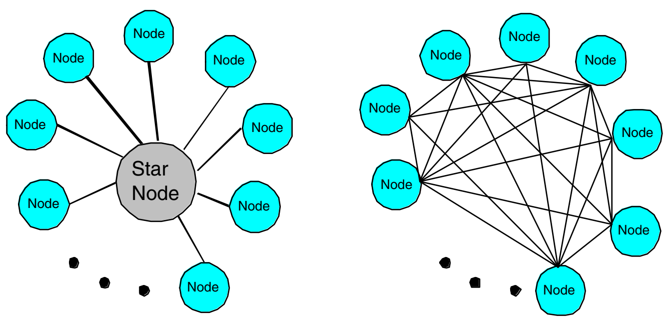

Fig. 1. Star and full mesh topology of ATCA backplane.

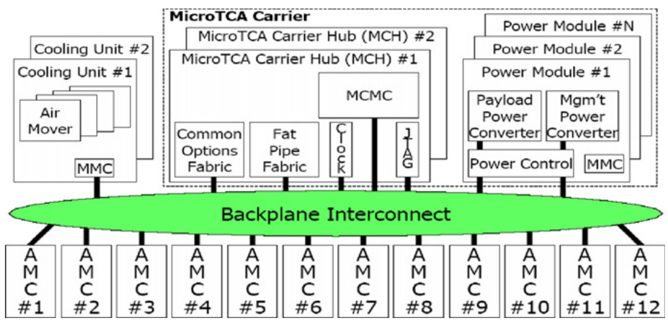

Fig. 2. μTCA system architecture.

ATCA system can support switching protocols and point-to-point protocols. There are two main configurations of the backplane shown in Fig. 1: star topology and mesh topology. In the star topology all nodes (slots of the ATCA shelf) are connected to one node, called the star node. In the mesh configuration each node is connected to all others in the shelf. Star topology is the simplest topology while mesh is the most complicated but also the most flexible. The ATCA system support also rear IOs via an optional Rear Transition Module (RTM). In the μTCA system only switched protocols are supported and all interconnection is handled via the μTCA Carrier Hub (MCH). Point-to-point connections are not possible and there in no support yet for rear IO. The architecture of μTCA is shown in Fig. 2.

3. xTCA for instrumentation

xTCA was designed to address first the telecommunication market. Several CPU, DSP boards, switches have already been available for several years in the ATCA or AMC form factors. xTCA seems very attractive due to its strong infrastructure but lacks some important features and broad vendor support for instrumentation.

3.1. A few xTCA recent laboratory developments

The first attempt by the nuclear physics community to design xTCA instrumentation seems to have been done by the Advanced Gamma Tracking Array (AGATA) Trigger and DAQ system starting in 2005 [3]. Today, the PANDA experiment at FAIR is an example of development of a large modern architecture for trigger and Data acquisition fully designed using ATCA [4]. Recently, SLAC has embarked on a research project intending to explore the suitability of the ATCA platform as a configurable solution for a variety of high-speed data acquisition needs for future large detectors like for the ILC. Two ATCA boards have been designed

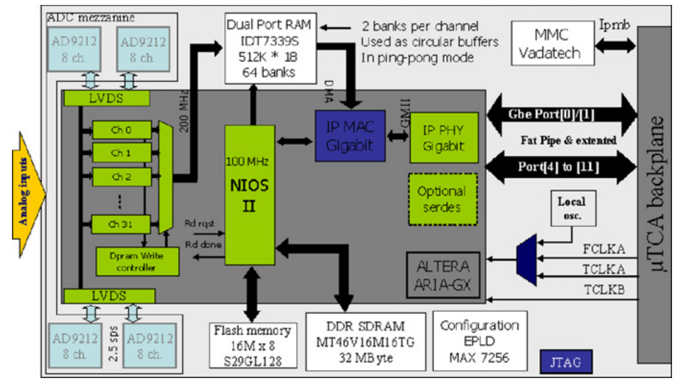

Fig. 3. AMC-ADC board developed for T2K experiment.

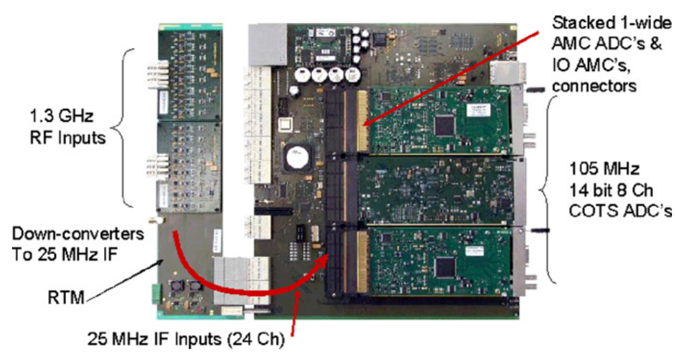

Fig. 4. The carrier board, RTM and AMC modules for LLRF control system for EU_XFEL.

using system on a chip technology, a reconfigurable cluster computing element with memory and a cluster interconnect hub switcher, to achieve multiple 10 Gb/s lanes and ~0.5 TB/s system data throughput [4].

The T2K 2 km Liquid Argon Detector read out is also an example of a large system using μTCA [5]. More than 10,000 analog channels must be digitized. For this experiment an AMC with 32 ADC digitizer channels, 1.5 MHz and 10 bits in under development. The complete system will consist of 34 μTCA racks (9 slots). Data acquisition is done over Gigabit Ethernet output through the backplane. The block diagram of this AMC board is shown in Fig. 3.

At DESY the Low Level Control System for the European-XFEL is under development [6]. The system will consist of 60 ATCA crates (shelves), equipped with ATCA carrier blades, AMC and RTM modules. Analog RF signals are connected to the RTM modules, then down-converted to an intermediate frequency 54 MHz, routed via the carrier board to AMC slots and then digitized by AMC-ADC modules. The carrier board with connected RTM modules and AMC modules is shown in Fig. 4. The system has to process more than 3000 analog channels within 500 ns.

3.2. xTCA development in industry

TEWS Technologies [7] has developed according to DESY requirements an AMC-ADC module TAMC900 (8 channels, 14 bits, 105 MHz sampling frequency) (Figs. 4 and 5). It is one of the first modules available on the market designed for physics. TEWS also offers AMC Adapters to support its line of Industry Pack (IP) modules. These industrial speed devices are already used broadly in physics machine slow control systems. VADATech is another company offering a broad range of AMC products,

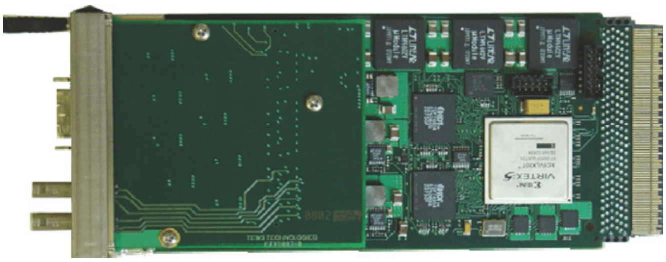

Fig. 5. TAMC900 AMC-ADC board (version with front panel inputs).

including some high speed digitizers. A half dozen companies are offering μTCA shelves that are being evaluated for physics use, such as Elma, Kontron and Performance Technologies.

4. xTCA for physics committee

Following several ATCA workshops for physics it was decided to form an xTCA for Physics Coordinating Committee under PICMG to pursue developing extensions to the standards for physics. The Coordinating Committee was formed in March 2009 and two Working Groups have been added for Hardware and Software issues. The main goals are to define new standards for rear IO for both ATCA and μTCA; to define lines for distribution of fast timing and synchronization clocks, and to define desired protocols, all features aimed at encouraging the physics community to collaborate on interoperable designs that can be supported by industry and shared among the participants.

Acknowledgments

We would like to thanks all the colleagues who gave input to this introductory talk: R. Downing (SLAC consultant), W. Kuehn (Geissen), Z. Liu (IHEP), M. Nomachi (Osaka), V. Pavlicek (FNAL), K. Rehlich (DESY), and S. Simrock (DESY).

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