FPGA BASED, FULL-DUPLEX, MULTI-CHANNEL, OPTICAL GIGABIT, SYNCHRONOUS DATA TRANSCEIVER FOR TESLA TECHNOLOGY LLRF CONTROL SYSTEM

Krzysztof T. Pozniak, Ryszard S. Romaniuk,
Wojciech Jalmuzna, Krzysztof Olowski, Karol Perkuszewski, Jerzy Zielinski

ELHEP Group
Institute of Electronic Systems, Warsaw University of technology,
Nowowiejska 15/19, 00-665 Warsaw, Poland

Krzysztof Kierzkowski

Institute of Experimental Physics, Warsaw University
Hoza 69, 02-093 Warsaw, Poland

ABSTRACT

It may be predicted now, even assuming very conservative approach, that the next generation of the Low Level RF control systems for future accelerators will use extensively such technologies like: very fast programmable circuits equipped with DSP, embedded PC and optical communication I/O functionalities, as well as multi-gigabit optical transmission of measurement data and control signals.

The paper presents the idea and realization of a gigabit synchronous data distributor designed to work in the LLRF control system of TESLA technology based X-ray FEL. The design bases on a relatively simple and cheap FPGA chip Cyclone. Commercially available SERDES (serializer/deserializer) and optical transceiver chips were applied. The optoelectronic module is embedded on the main LLRF BMB (backbone mother board). The MB provides communication with the outside computer control system, programmable chip configuration, integration with other functional modules and power supply. The hardware implementation is here described and the used software for BER (bit-error-rate) testing of the multi-gigabit optical link. The measurement results are presented. The appendix contains a comparison between the available protocols of serial data transmission for FPGA technology.

This TESLA Technology Report is a partial contribution to the next version of the SIMCON system which is expected to be released this year. The SIMCON, ver 3. will contain 8 channels and multi-gigabit optical transmission capability.

Keywords: Super conducting cavity, FPGA, VHDL, serdes, optical link, Altera, Cyclone, TESLA technology, LLRF systems, Bit Error Rate, multi-gigabit transmission, accelerator control systems, distributed measurement and control systems,

**FPGA based, full-duplex, multi-channel,
optical gigabit, synchronous data transceiver
for TESLA technology LLRF control system**

CONTENTS:

1   INTRODUCTION

The LLRF control system is responsible for a precise repetitive loading of the cavity with the EM high power energy and for the EM field stabilization. A single channel system works with a single cavity. The 8 channel (or 10 channel system under preparation) system works with a single TESLA module (ACC) of 8 cavities. The modular electronics design predicts now work with up to 32 cavities per LLRF board (addressing a group of four SC modules).   The system should be able, however, by hardware stacking or proper data concentration, to work with much larger number of modules, as predicted in the X-Ray FEL. The multichannel system should provide all functionalities, individually for all cavities and for the vector modulator. The control RF signals (1,3 GHz) from particular cavities are downconverted in frequency to 250 kHz and demodulated. The I and Q values of the EM field are recovered from this signal. Basing on these measurement results, a very fast DSP algorithm calculates the new values of I and Q for control purposes via the vector modulator [1,2].

In the above context, the LLRF system may be represented as a multichannel, synchronous and pipelined hardware and functional concentrator. The feature of the measurement system to be multichannel stems from the readout needs from many signal sources simultaneously (particular cavities). The synchronous regime of work provides simultaneous processing of relevant data for all channels inside the same time slot. The pipeline architecture provides successive data processing from the A/D conversion, via a number of DSP stages, to the eventual DA conversion, leading to the klystron control.

The extent of the functional concentration in the system includes the DSP module. This stems from the currently used algorithm which chooses the control values on the base of the input data. As a consequence, the aim of the hardware concentration is to group a number of physical signals in a single DSP module. Thus, the LLRF system can be considered as a distributed hardware concentrator networked by fast, synchronous optical data links.
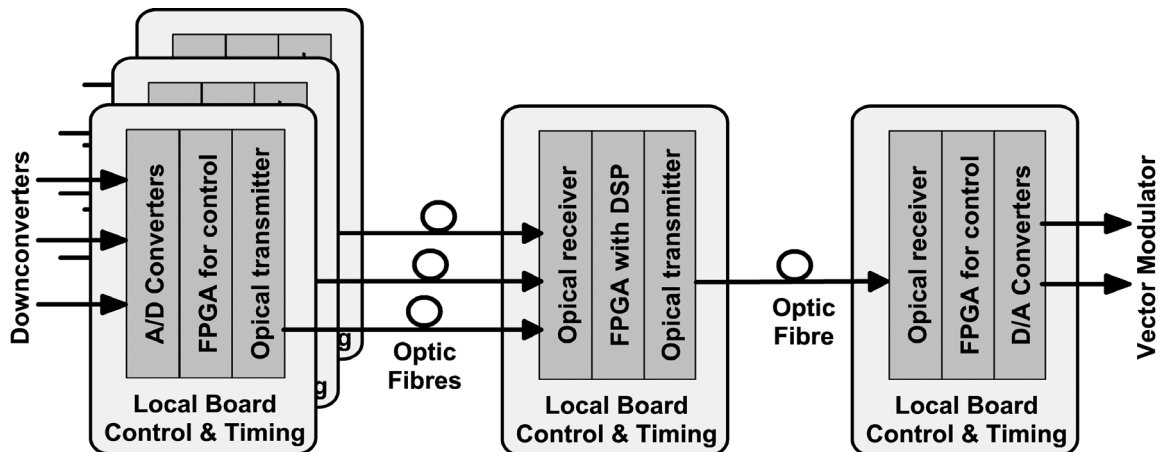
Fig. 1. General hardware model of distributed structure for TESLA LLRF control system

Fig. 1 presents a general hardware model of the distributed LLRF system. The system bases on the FPGA chips, which are connected by optical network. This novel approach was analyzed in comparison with the classical solutions. The initial conclusions are that the networked (distributed) model allows for easy system structure modification in reference to scalability (number of channels), distribution, reach and the extent of signal processing. Optical links connect FPGA boards of different functionalities in this solution. The hardware modifications of the system concern only its particular parts, like single boards.

This paper describes in details the constructed module of optical transceiver. The module works at the data rate of 1,6-2,4 Gbps and cooperates with the SERDES chip TLK2501 by Texas Instruments [10]. The serdes and optical transceiver are controlled by FPGA chip – Cyclone by Altera [14]. The module possesses two nondependent transmission channels. Such configuration makes of this module a cheap and versatile optoelectronic network RRR node (regeneration, reclocking, repeating). Using a number of nodes, a network can be created between functional FPGA PCBs. This idea allows either to build a concentrated or distributed LLRF system for accelerators [8] basing on TESLA technology solutions. Now the optoelectronic transceiver is an integral part of a modular version of the LLRF control system tested for the VUV FEL

Since the development of used FPGA chips in our solutions to LLRF systems is very fast, we decided to include, in this paper, an updated comparison of the gigabit communication interfaces applied in these chips. The aim is to apply direct coupling of the optoelectronic transceiver to the FPGA chip to minimize the overall system latency. The comparison embraces hardware solutions (discrete chips or inbuilt blocks) and developmental tendencies as well as the used efficient transmission protocols. The comparison results in conclusions on applications of particular optoelectronic solutions in the LLRF control system

2   HARDWARE STRUCTURE OF OPTO MODULE

A general hardware structure of „OPTO" module was presented in fig. 2. The module possesses two nondependent, duplex, optical, gigabit transceiver channels (see chapter 2.1.). The control of optical channels and cooperation with the LLRF hardware platform is done by the FPGA chip (see chapter2.2.).
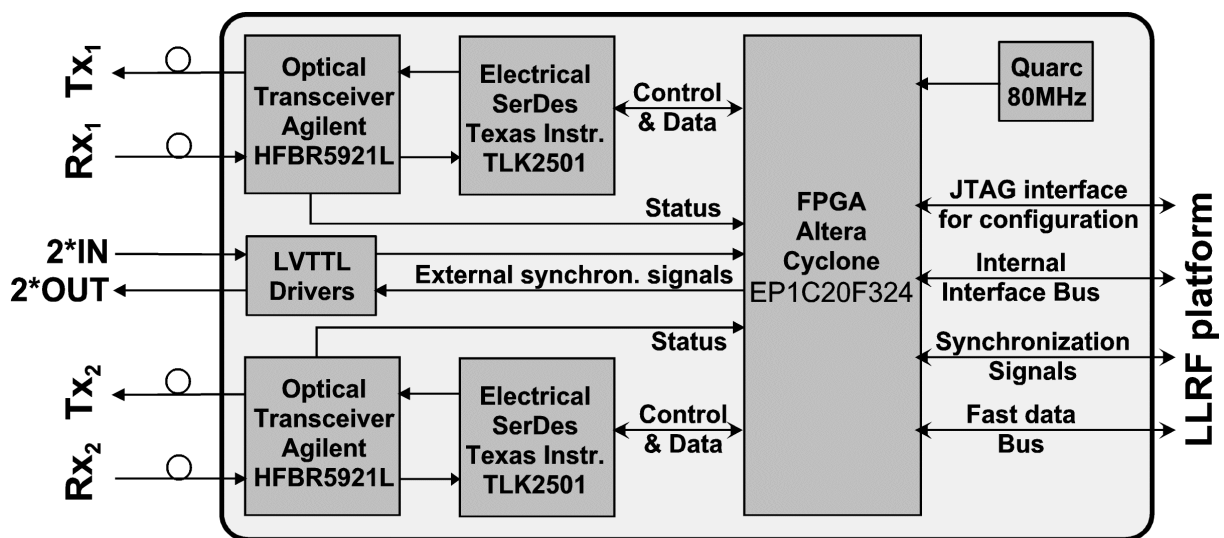
Fig. 2. General hardware structure of „OPTO" module

Fig. 3 presents the construction of the PCB for the OPTO module. Positions of the major functional components are marked. The OPTO module was designed as a DB (daughter board) to be connected to the main LLRF PCB. The OPTO board is inserted into the **D** slot on the LLRF MB [8]. This situation was presented in fig. 4. This kind of positioning makes out of the LLRF hardware platform a functional concentrator designed for fast transmission and optical data redistribution

Fig. 3. Details of PCB construction for the multi-gigabit OPTO module

Fig. 4.   VME crate based test and measurement set-up with the OPTO module embedded in the main LLRF control system PCB.

2.1 Gigabit duplex optical channel

The OPTO module possesses two duplex optical channels. The data serializing circuit uses the TLK 2501 serdes chip (by TI) [10]. The optical transceiver uses the O/E HFBR-5921L chip (by Agilent) [11].
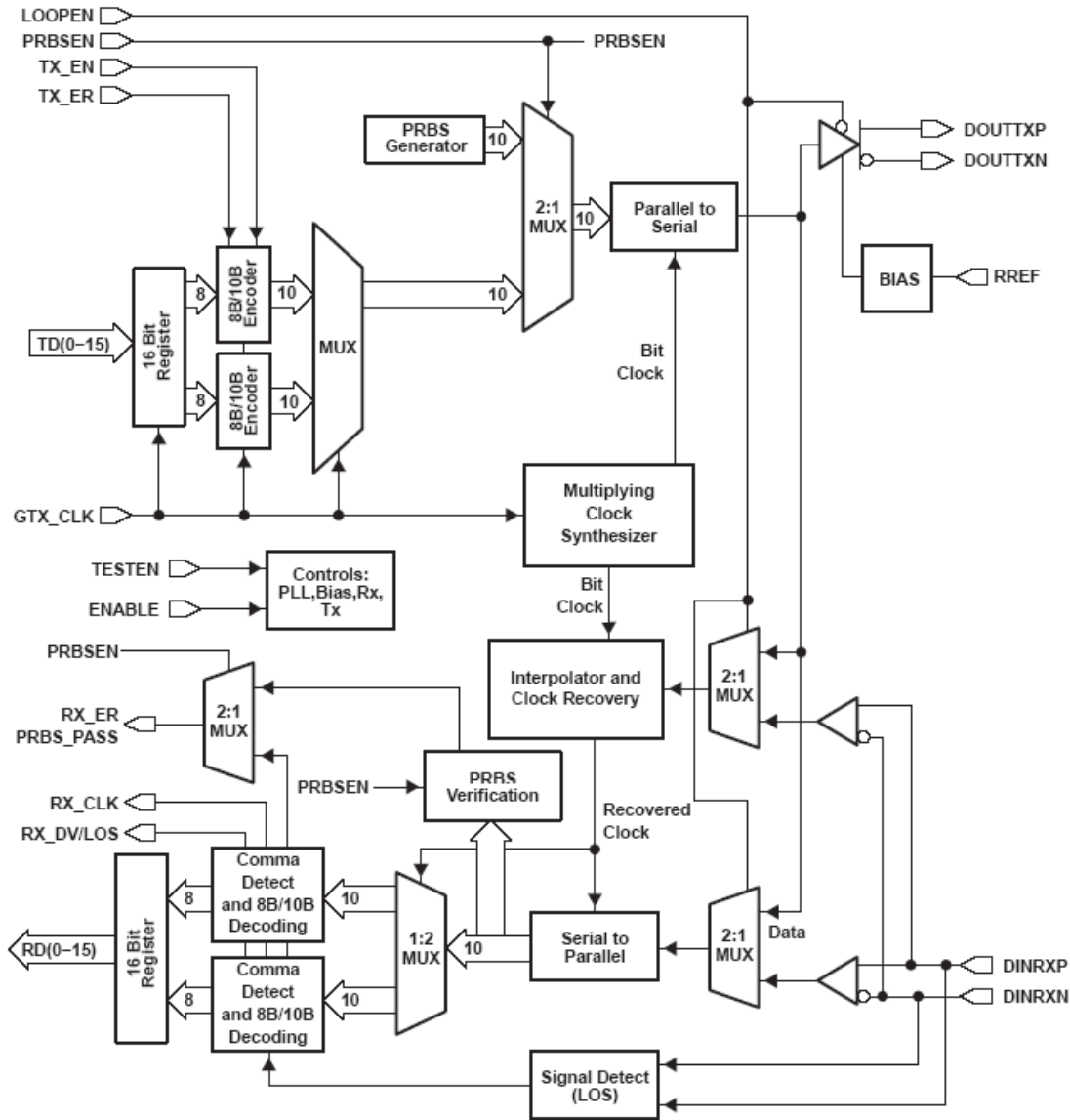
Fig. 5. Internal, electrical schematics of TLK2501 SERDES chip (TI).
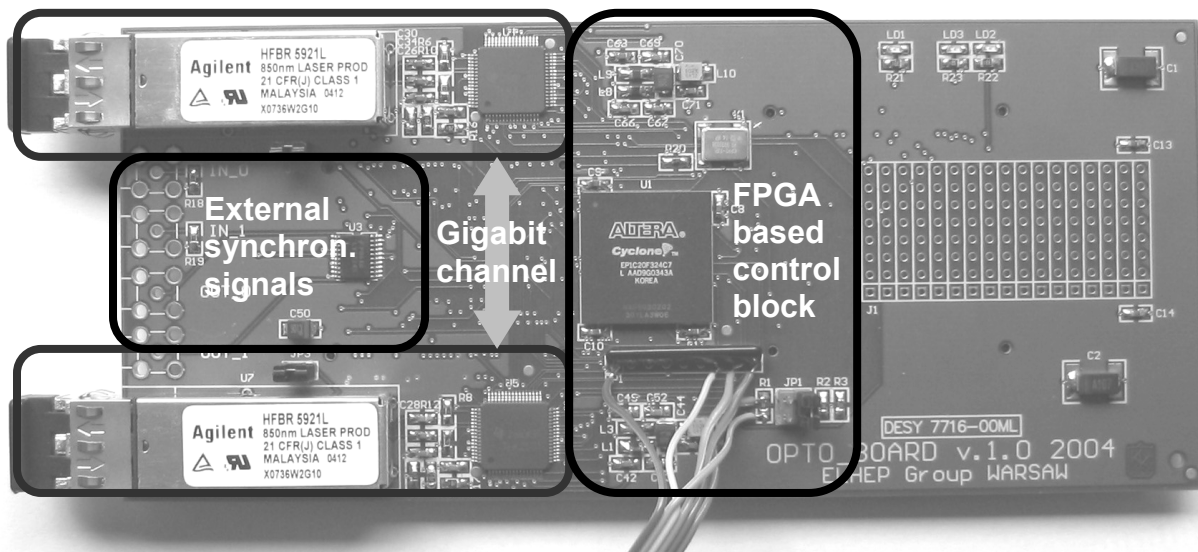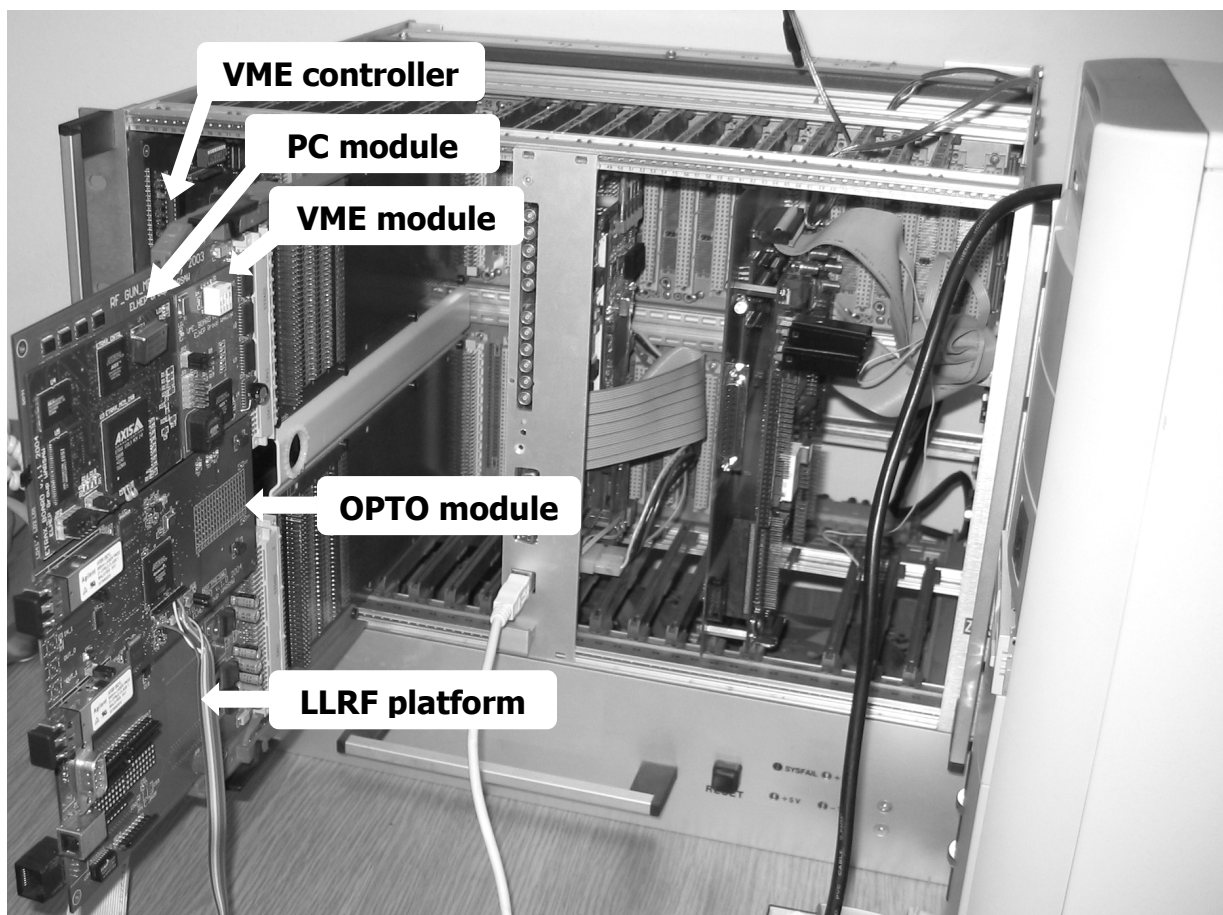
The TLK 2501 is a transceiver chip, designed for serial data transmission with the rate of 1.5 to 2.5 Gbit/s. It enables either a direct, point-to-point electrical transmission or cooperation with optoelectronic transceivers pigtailed with fibers. The diagram of TLK chip was presented in fig. 5. The chip has inbuilt several features, like: 8b/10b coding and decoding (see the Appendix A), comma alignment and line synchronization. The TLK2501 may work with the base clock signal in the range of 75 – 125 MHz. The internal PLL circuit does the synthesis of the TX clock signal for the gigabit transmission. The circuit provides clock signal recovery from the received data. It also discovers the loss of the signal. The latency of the TX circuit is 34 – 38 of the sent bits. This is equivalent to 4 periods of the base clock. The latency of the RX circuit is 76 – 107 of the received bits. This is equivalent to 9 periods of the base clock.

Fig. 6. Internal block diagram of optoelectronic converter chip HFBR-5921L by Agilent.

The optoelectronic duplex transceiver HFBR-5921L is designed to build an optical 850 nm channel for data rate of 2.125 Gb/s. It is compatible with the Fiber Channel standard. The internal structure of the transceiver is presented in fig. 6. The transmitter uses a VCSEL laser. The laser diode is controlled by a circuit converting the digital differential voltage signal to the analog current ex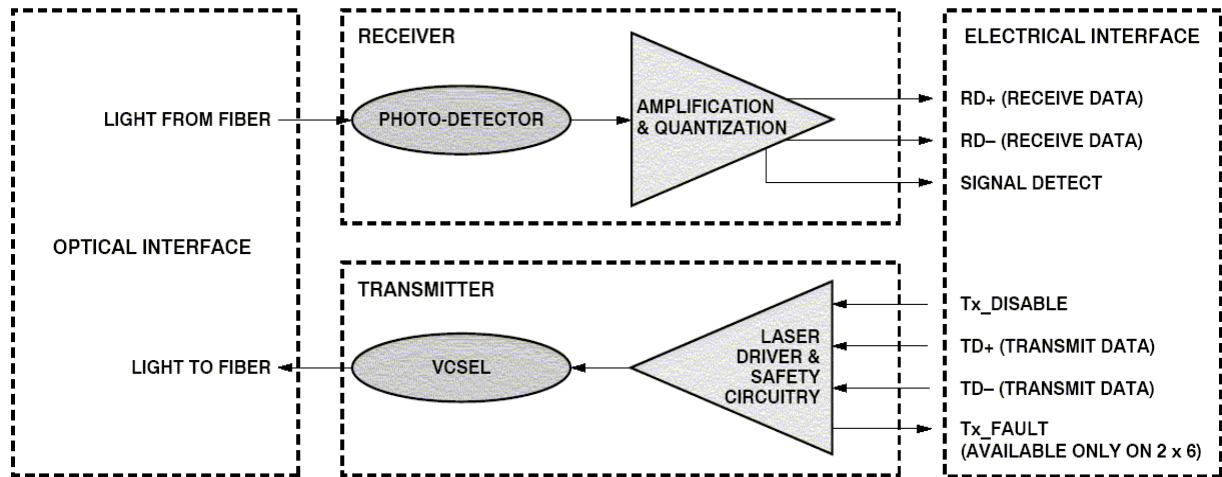citation of the diode p-n junction. The reception of the optical signal is provided by PIN photodiode. The photodiode cooperates with a transimpedance amplifier and a quantization circuit. Multimode optical fibers were used for the transmission tests. The fiber data were: core diameter either 50μm, step index or 62,5μm also step index. The fibers were terminated with the LC connectors. The nominal transmission span was 300 and 150 m, for 2,125Gbps and both types of the fibers. The nominal transmission span was 500 and 300 m for 1,0625GBd. The HFBR-5921L chip is powered with 3,3 V. The rise and fall time in the TX is 150 ps. The rise and fall time in the RX is 250ps. The extinction ratio of the TX is 9 dB.

2.2   OPTO module control with FPGA chip

The OPTO module contains a programmable matrix. There was applied the EP1C20 chip from the Altera Cyclone family of FPGAs. It is a family of fast and cheap chips possessing a considerable number of LCELLS. The basic parameters of the Cyclone family chips are gathered in table 1.

CYCLONE chip fmily:	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
Number of LCELLs	2,910	4,000	5,980	12,060	20,060
Memory in [bit]	59,904	78,336	92,160	239,616	294,912
Number of PLL	1	2	2	2	2
Max. Number of I/O pins	104	301	185	249	301

Tab. 1. Basic parameters of the CYCLONE FPGA chip family (by Altera).

Application of the largest chip from the Cyclone family provides 20k of logical components. This is enough, in many cases, to implement even sophisticated hardware solutions. The chip has nearly 30kB of configurable SRAM memory designed to work in data buffers and acquisition, LUT conversions, FIFO memory, etc. The internal clock of the matrix may work at the rate of 80 – 120 MHz. This rate is sufficient to realize the synchronous logical circuits cooperating directly with the TLK2501 chips. The internal PLL blocks enable appropriate frequency multiplication and phase change of the clock signal.

The FPGA CYCLONE EP1C20 chip is directly connected with:

- JTAG interface is designed to configure and test the FPGA matrix. The JTAG driver is located in the FPGA chip of the LLRF platform controller [8],

- *Internal Interface* bus [3] provides communication with the upper layer computer control network via the interfaces of VME [8,9] and Ethernet [7] positioned on the LLRF platform. The Internal Interface bus provides a 32-bit address bus and 32-bit data bus.

- Synchronization signals of the LLRF platform. The source of these signals may be the platform controller or other module situated in **A-C** slots of the LLRF MB,

- Fast 32-bit data bus connected directly with the FPGA chip of the LLRF platform MB. It enables data redistribution to other sots of the platform,

- Functional circuits of both multi-gigabit optical transmission channels. The FPGA matrix provides full control and work monitoring of the channels, TX and RX data distribution,

- Two external synchronization signals from the LLRF system provided in the LVTTL standard. To assure the proper safety level, the signals are initially buffered,

- Two output synchronization signals, of general purpose, realized in the LVTTL standard. To assure the proper safety level, the output signals are buffered.

There are connected necessary signals to the Cyclone matrix from all of the functional blocks of the Opto module and from the slot **D** of the LLRF platform. The matrix concentrates all required control, diagnostics, monitoring and data acquisition functions. A full, programmable reconfiguration ability of the matrix enables implementation of a variety of hardware applications realized by the Opto module. The next chapter presents example of an application for bit error rate measurement of optical transmission. The quality and reliability of the optical channels was estimated basing on these measurements.

3   APPLICATION FOR BER MEASUREMENTS

An application was designed and realized to estimate the quality of the optical communication channels using the above mentioned components. The major aim to measure the BER coefficient in optical channels was to investigate the ultimate properties of the networking sub-system and its potential to be used for construction of the distributed LLRF system. It is to be emphasized that the optical backbone network based solution is a completely new approach to the LLRF control system design. The presented application was tested not only for the basic properties but also for the following functionalities and features:

- Design and tests of the control algorithms and their remote execution via the ulrafast TX and RX electrical channels of the TLK2501 chip; synchronization of the received data with the system clock, monitoring of the current state of synchronization;

- Evaluation of the costs of logical implementation and the rate of internal clock of the application in the FPGA chip, depending on the used class of functional solutions,

- Checking the functioning of the communication in the *Internal Interface* bus [3] and with the LLRF platform and the computer control system as well as the control software, internal registers, embedded memory of the FPGA chip,

- Design and tests of parameterized components library, prepared in VHDL and designed for functional applications of the LLRF control system,

The extent of work was: design of hardware implementation in VHDL (chapter 3.1.), design and tests of control software in the MatLab environment, integration of the software with communication layer of the *Internal Interface* bus (chapter 3.2.). The II bus is a proprietary solution of the ELHEP Group.

3.1 Hardware layer application for Cyclone FPGA chip

The application of hardware layer implemented in Cyclone (FPGA EP1C20F324C7 ALTERA) consists of two parts. The first one embraces the service of communications with the *Internal Interface* (*II*) and programming of the work area (see chapter 3.1.1.). The second one realizes the executable part of the measurement process for the BER coefficient (see chapter 3.1.2.). The block diagram of the hardware layer implemented in the FPGA chip is presented in fig.7.
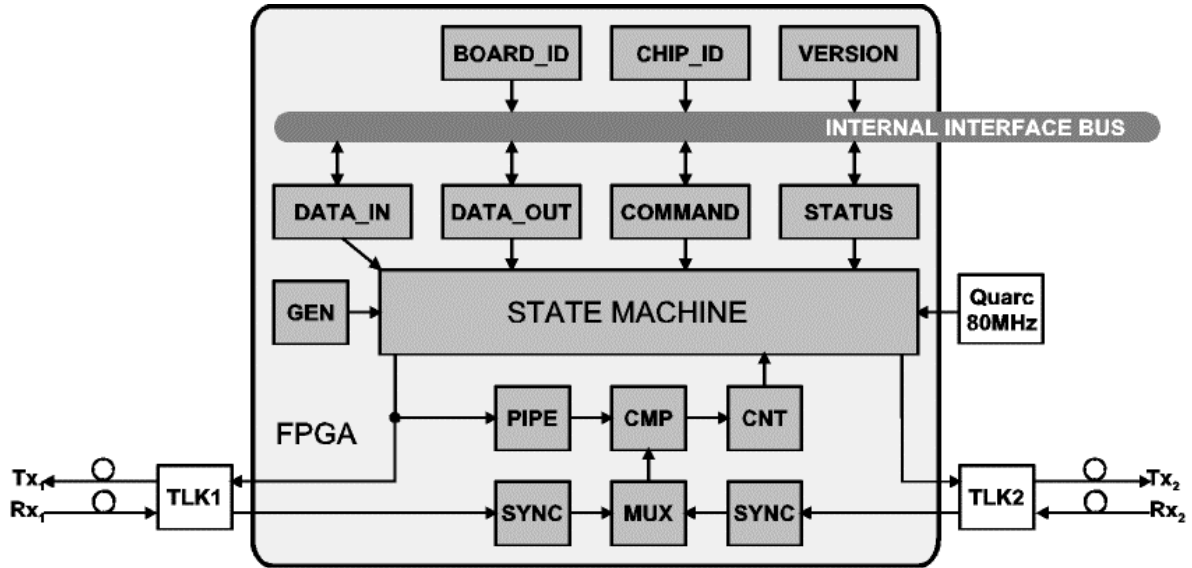
Fig. 7. Block diagram of hardware layer implemented in the Cyclone FPGA matrix

The real-time control of the measurement process is realized by the *STATE MACHINE* block. Programming of the work parameters of the hardware layer and current monitoring of the process functionality is provided by the communication layer. The *STATE MACHINE* enables realization and control of the measurement algorithm. The algorithm itself is described in chapter 3.1.3.

3.1.1 Communication layer

The control of transmission parameters and monitoring of the testing process is done via the programmable access to the appropriate configuration registers of the proprietary *Internal Interface (II)* bus. These registers of the working area were gathered in table 2.

Register nama	Address	Value	Function
WORD_BOARD	0	(ASCII) „OPTO"	Board ID
WORD_CHIP	1	(ASCII) „ABCD"	Chip ID
WORD_VERSION	2	(HEX) 10000001	Software version
WORD_COMMAND	3	-	Command
WORD_DATA_IN	4	-	Input data
WORD_DATA_OUT	5	-	Output data
WORD_STATUS	6	-	Status word

Tab. 2. Registers of the work area

The first three registers (*WORD_BOARD*, *WORD_CHIP* and *WORD_VERSION*) have the values set on the level of VHDL code and possess only informative and identification character. Reading out of their proper current content (as shown in table 2) confirms the right

configuration of the FPGA chip and efficient communication via the *II* bus. The rest of the registers is programmable according to the specification shown below:

- The register WORD_COMMAND enables operations of particular functions of the block *STATE MACHINE*. This is done via executing a command in a form of numerical value:

  ✓ **CMD_NONE**: the machine goes to the state IDLE. All signal values are preserved with exception of the *RESET*, which assumes value 0,

  ✓ **CMD_RESET**: this state erases the contents of the counters and the queues. Both TLK2501 chips are set to IDLE state and transmit only synchronization signals,

  ✓ **CMD_SEND_REG**: the command sends the contents of the register *DATA_IN* to the input of *TLK1* block and sets the work mode to the transmission of regular data,

  ✓ **CMD_SEND_GEN**: the command sends the current contents of the *GEN* generator to the input of *TLK1* block and sets the work mode to the transmission of regular data,

  ✓ **CMD_SET_TLK_1**, **CMD_SET_TLK_2**: the command decides of the channel configuration. For *CMD_SET_TLK_1* the TLK2 circuit gets non-active, and transmission tests are done only with the *TLK1*. The command *CMD_SET_TLK_2* configures *TLK1* only to the transmit work mode. *TLK2* assumes the role of a receiver and the tests are done between two TLK chips,

  ✓ **CMD_OUTPUT_0**, **CMD_OUTPUT_1**: this command controls the multiplexer. The multiplexer decides of the contents of *DATA_OUT* register. After the command *CMD_OUTPUT_0* is executed, the data from the output of the appropriate *TLK* block are placed in this register. The command *CMD_OUTPUT_1* inserts to this register the current status of the error counter *CNT*,

  ✓ **CMD_CLK_SRC_1**, **CMD_CLK_SRC_2**: the commands choose one of two ways of the clock synchronization,

  ✓ **CMD_SET_DELAY**: the command sets the length of the delay queue. This parameter is called by the *DATA_IN* register.

- The input parameters are called by the WORD_DATA_IN register.

- The results of the commands are inserted in the register WORD_DATA_OUT.

- The register WORD_STATUS enables the current work monitoring of the TLK2501 and HFBR5921L chips, according to the following specification:

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status SYNC	Status TRANS2	Status TRANS1	Status TLK2	Status TLK1

  ✓ **Status TLK1/TLK2** gathers aggregated transmission error states for particular TLK2501 chips [10],

  ✓ **Status TRANS1/TRANS2** represents signal states *TRANS_SD* (signal detect) of particular transceivers [11].

  ✓ **Status SYNC** is a flag of the clocks synchronization state.

3.1.2 Functional structure of BER measurement channel

Functional structure of the channel for the BER measurement coefficient is presented in fig. 7. It consists of a few separate functional blocks. These blocks are described in the following chapter. These circuits are directly controlled by the *STATE MACHINE* according to the parameters set by the user, via the communication layer of the system.

The measurement channel of the BER calculates the number of bits which are not in agreement with the pattern generated by the *GEN* block. The pattern is generated by a 16-bit

wide counter. The width of pattern is equal to the number of word bits in optical transmission channel.

The TX latency, which stems from the data distribution via the optical link, is made equivalent to the pattern due to application of the programmable delay block *PIPE*. The applied optical fiber of 5 m in length introduces 11 periods latency of the system clock. The clock works at 80MHz. The latency stems from serialization, optical transmission and deserialization processes. The maximum range of allowed latency was assumed to be 31 periods of the clock.

The choice of the received data stream is performed by the *MUX* block. The data stream is compared with the pattern data in the verification block *CMP*. The comparison relies on the nondependent XOR operations for each bit of the stream. The successful comparison generates the output '0', while the non-successful '1'.

The error counter *CNT* bases on 16 individual counters, each is 32 bits wide. Each counter counts nondependently the errors of particular bits in the transmitted data word. This gives a solution of BER evaluation which is nondependent for every bit. The aggregated value of the BER coefficient is expressed by the following dependence:

$$BER_{TOTAL} = \frac{\sum_{i=1}^{16} CNT_i}{T} \tag{1}$$

The process of data comparison with the pattern requires the full received data synchronization with the phase of the main clock of the Opto module (*CLOCK*). The data output from the TLK2501 chip (*RX DATA*) is synchronized with the recovered clock (*RX_CLOCK*). Phase shift between the clocks is constant but may assume an arbitrary value from the range <0;2Π>. The data synchronization block *SYNC,* presented in fig. 8, enables the change of data timing from the receiver clock to the main clock.

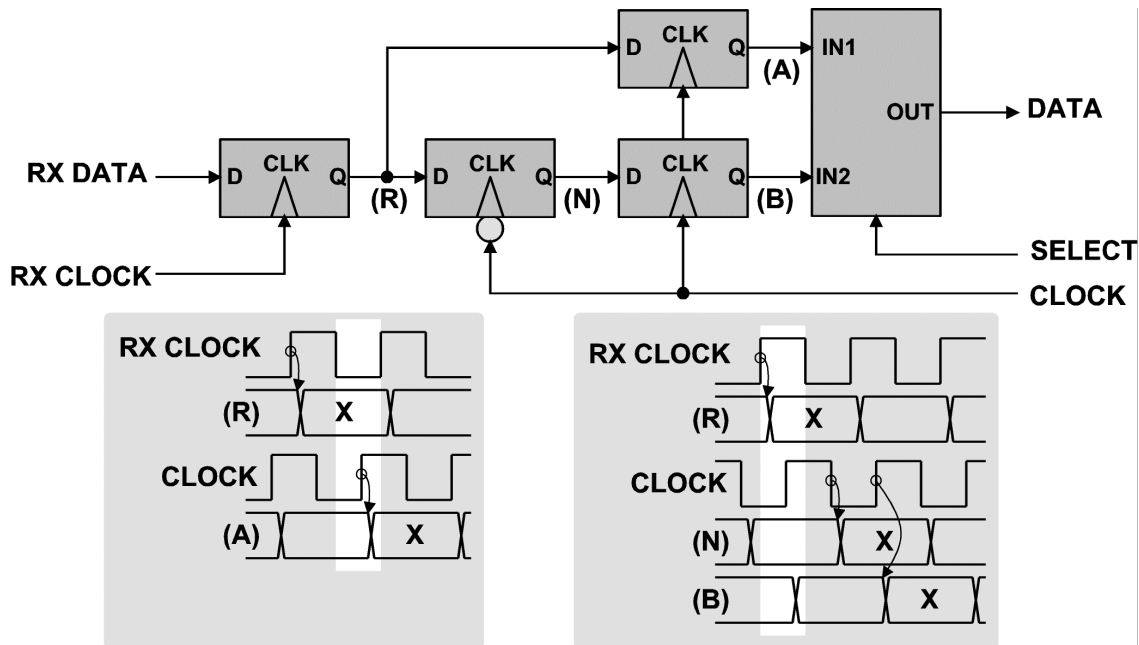Fig. 8. Block diagram of synchronization circuit for data received via optical link. Two options of synchronization: direct (left time diagram), indirect (right diagram).

There are shown two options of synchronization. The left diagram presents direct synchronization – data rewriting (signed as 'X') from the RX register (R) to the phase register (A). The range of phase for this option is marked by a white slot.

The right diagram presents indirect synchronization. The X data is rewritten from the RX register (R) to the intermediate register (N). The N register is timed with the falling edge of the main clock. The closest rising edge of the main clock signal causes the data to be rewritten to the main register (B). The phase range for this option was marked as a white slot. The choice of options is realized by the programmable multiplexer controlled by the *SELECT* line.

3.1.3   Measurement algorithm of BER

The measurement algorithm of BER is performed by the *STATE MACHINE* block, basing on the programmably set parameters. The successive steps of software initialization and automatic realization of the algorithm is presented in fig. 9.
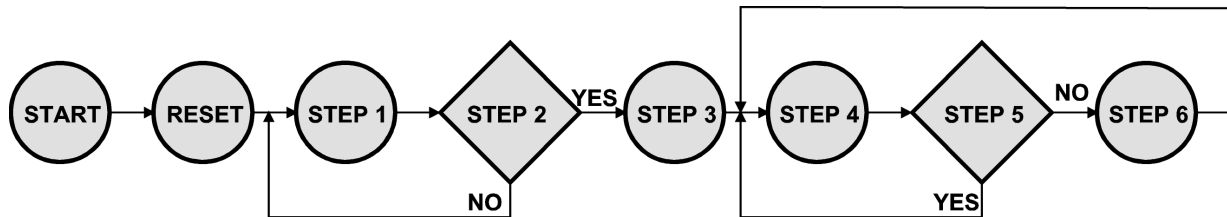
RESET	All counters are zeroed, the contents of queue is erased, dimension of queue is 0
STEP 1	increase GEN, increase dimension of the queue of 1, shift queue, state of GEN => queue, send state of GEN via TLK1
STEP 2	Receive data from TLK2, if received data = data at queue output?
STEP 3	reset GEN to zero, reset TLK to state IDLE
STEP 4	Shift queue, increase GEN, status GEN => queue
STEP 5	If data received from TLK2 = output data on queue ?
STEP 6	Increase error counter for erroneous bits

Fig. 9. Succession of logical steps for measurement algorithm of BER

- *STEP 1* and *STEP 2* enable the user programmable setting of the appropriate dimension of the queue. There are done the following operations from the level of communication layer:
  - ✓ A command CMD_RESET is sent to the COMMAND block,
  - ✓ A command CMD_SET_TLK2 is sent to the COMMAND block; It decides that the TLK2 has to assume the role of a receiver, and the TLK1 a transmitter,
  - ✓ A command CMD_SEND_CNT is sent to the COMMAND block; The transmission is started, the status of the counter changes with each clock period,
  - ✓ A required size of the queue is sent to the block DATA_IN; next, the command CMD_SET_DELAY is sent to the block COMMAND; The queue is set to the desired size. If this size is appropriate, the fourth bit in the STATUS register (status SYNC) assumes the value of 1. CAUTION: in certain cases, to obtain appropriate synchronization, it is necessary to regulate the synchronization system clocks using the CMD_SET_CLK command.

- From the phase of *STEP 3,* the automatic measurement process begins. The values of CMD_RESET and next CMD_SEND_CNT are introduced to the register COMMAND. From this moment the TLK1 sends the status of the counter GEN. After reception of this value by the TLK2, it is compared with the output of the queue.

The current status of work of the hardware layer is reported by the STATUS register. This includes: loss of synchronization, error discovery in coding, other errors reported by the TLK circuits or transceivers.

In order to obtain the current status of the measurement process it is necessary to introduce a command CMD_OUTPUT_1 to the register COMMAND. It causes that the number of errors for a particular bit is rewritten to the register DATA_OUT, in agreement with the addressing in the register DATA_IN.

3.2 Control application in MatLab environment

In order to control and automate the measurement process of BER, an application was designed in MatLab 6.5 environment. It realizes communications with the OPTO module via the *Internal Interface* bus. In the result, the user has access to an integrated, interactive control panel. The panel was shown in fig. 10. The most important control functionalities are numbered and described in table 3.
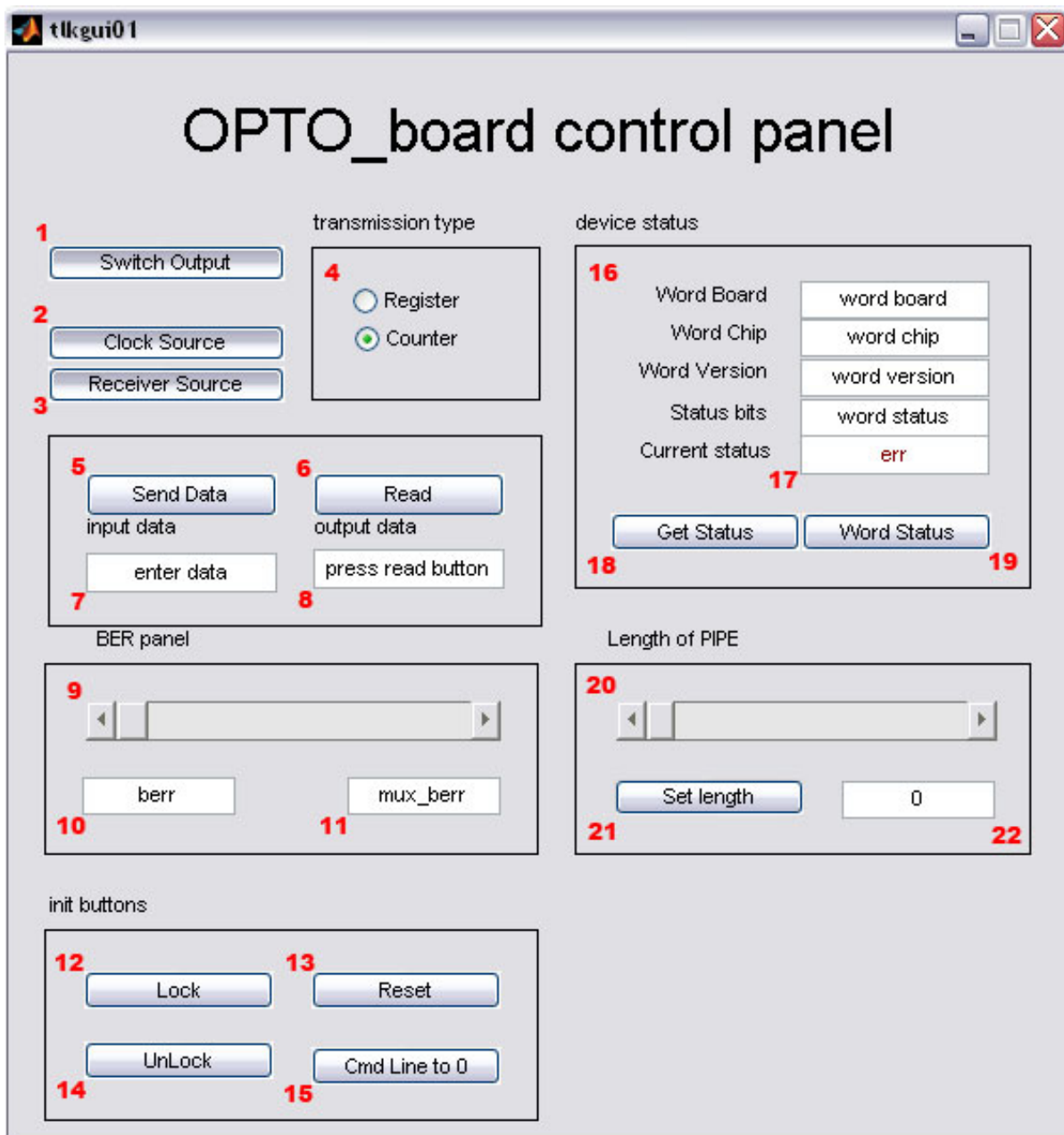

Fig. 10. Control panel *tlkgui01* for measurements of BER

Tab. 3. Control functions of application for BER measurements
using the multi-gigabit OPTO module

Position	Name	Function
1	*Switch Output*	**Bistable button/switch (on/off)**
		Choice of kind of output signal for MUX block (chapter 3.1.)
2	*Clock Source*	**Bistable button (on/off)**
		Choice of clock signal source: simple or shifted in phase (chapter 3.1.2.)
3	*Receiver Source*	**Bistable button (on/off)**
		Choice of received signal source, determined by multiplexer, MUX is pointing to a constant register or a counter,
4	*Register/Counter*	**Window for choice of data source to be sent during data transmission tests**
		Accessible functions:
		✓ *Sending contents of register (see positions 5 and 7)*
		✓ *Sending of current status of counter*
5	*Send Data*	**Button for transmission start**
		Choice of transmitted data is from a list- position 4
6	*Read*	**Single state button**
		Readout of current value of register determined by position 3
7	*Enter Data*	**Single state button**
		Acknowledgement and sending data to register, data are written in the window in position 8
8	*Enter Data Text box*	**Dialogue window for sent data**
		Writing of to be sent data in decimal form to FPFA chip register; contents of this register is sent by pressing the button from position 5
9	*BER Multiplekser slider*	**Slider for the choice of counter of BER status for word bit**
		Choice of one of 16 counters is done by sliding to proper position. Number of chosen counter is in window from position 11. Simultaneously, counter status is displayed.
10	*BER Text Box*	**Window for BER status for chosen counter**
		Choice of counter is done by slider from position 9
11	*BER MUX Text Box*	**Window for the number of chosen position**
		Choice of counter is done by slider from position 9

Position	Name	Function
12	*Lock*	**Single state button**
		Calling the procedure „ii_lock", connection with server
13	*Reset*	**Single state button**
		Sets the initial status of module
14	*Unlock*	**Single status button**
		Calling the procedure „ii_unlock", disconnecting from server
15	*Cmd line to 0*	**Single status button**
		Setting CMD line status to zero (0)
16	*Device Status Text Boxes*	**Information windows**
		Windows showing current status of device
		✓ *board version*
		✓ *chip version*
		✓ *code version*
		✓ *status bits*
17	*Current Status Window*	**Information window**
		Presents current status of executed actions
18	*Get Status*	**Single state button**
		Readout of the device status to windows from position 16
19	*Word Status*	**Single state button**
		Reading of „status bits" for device to window from position 16s
20	*Length of PIPE Slider*	**Slider**
		Stting of queue length, the queue is of PIPE type (chapter 3.1.)
21	*Set Length*	**Single state button**
		Setting of PIPE value from dialogue window from position 22 (chapter 3.1.)
22	*Length of PIPE Text Box*	**Dialogue window**
		Sets value of PIPE (chapter 3.1.)

4 SUMMARY

This paper tries to describe synthetically the functional structure of a module for fast optical transmission. The module is designed for distributed data streams concentration in the TESLA LLRF control system. The module contains two duplex, parallel 2,4Gbps optical links. The idea of the transmition system was presented. The base PCB of the system was designed and practically realized. The OPTO board is compatible with the previous version of the base MB of the LLRF system (called LLRF platform). The following components were

used: optical transceiver – 1,6-2,4 GHz Agilent, serdes chip TLK2501 TI, FPGA chip Cyclone EP1C20F324C-7 Altera.

The OPTO module was tested in laboratory conditions and was integrated with the LLRF hardware platform. Transmission test were designed to prove the quality of RX and TX data. The automatic test procedures were inbuilt in FPGA chip as VHD, MatLab and C++ applications. The initial tests gave errorless data transmission of 1,6GHz random data stream for 48h, what results in BER $< 6.9*10^{-13}$.

5 REFERENCES

1. T.Czarski, R.S.Romaniuk, K.T. Pozniak "Cavity Control System, Models Simulations For TESLA Linear Accelerator ", TESLA Technical Note, 2003-09:
2. T.Czarski, K.T.Pozniak, R.Romaniuk, S.Simrock: "TESLA Cavity Modeling and Digital Implementation with FPGA Technology Solution For Control System Purpose " , TESLA Technical Note, 2003-28
3. K.T.Poźniak, K.Kierzkowski, R.S.Romaniuk: "Parameterized Control Layer of FPGA Based Cavity Controller and Simulator for TESLA Test Facility", TESLA Report 2003-30
4. W.M.Zabolotny, P.Roszkowski, K.Pozniak, R.S.Romaniuk, K.Kierzkowski, S.Simrock: "Distributed Embedded PC Based Control and Data Acquisition System for TESLA Cavity Controller and Simulator", TESLA Technical Note, 2003-34
5. K.T.Pozniak, R.S.Romaniuk, T.Czarski, W.Giergusiewicz, W.Jalmuzna, K.Olowski, K.Perkuszewski, J.Zielinski, S.Simrock "FPGA and Optical Network Based LLRF Distributed Control System for TESLA-XFEL Linear Accelerator, TESLA Technical Note, 2004-9
6. W. Koprek, P.Kaleta, J.Szewinski, K.T.Pozniak, T.Czarski, R.S.Romaniuk: "Software Layer for FPGA-Based TESLA Cavity Control System (Part I), TESLA Technical Note, 2004-10
7. P.Roszkowski, W.M.Zabolotny, K.Pozniak, R.S.Romaniuk, K.Kierzkowski, S.Simrock: "Prototype Implementation of the Embedded PC Based Control and DAQ Module for TESLA Cavity SIMCON", TESLA Technical Note, 2004-11
8. Krzysztof T. Pozniak, Ryszard S. Romaniuk, K. Kierzkowski: "Modular & Reconfigurable Common PCB-Platform of FPGA Based LLRF Control System for TESLA Test Facility" TESLA Technical Note, 2005-04
9. W. Petersen "The VMEbus Handbook"
10. "TLK2501 - 1.6 TO 2.5 Gbps transceiver", SLLS427A, Texas Instruments, 2000
11. "Agilent HFBR-5921L/HFBR-5923L Fibre Channel 2.125/1.0625 GBd 850 nm Small Form Factor Pin Through Hole (PTH) Low Voltage (3.3 V) Optical Transceiver", Data Sheet, Agilent Technologies, 2002
12. A.X.Widmer, P.A.Franaszek: "A DC-balanced, partitioned-block, 8b/10b transmission code", IBM Journal of Research and Development, vol 27, no 5, 1983, pp. 440-451
13. http://tesla.desy.de/doocs/ [DOOCS Homepage]
14. http://www.altera.com/ [Altera Homepage]
15. http://www.xilinx.com/ [Xilinx Homepage]
16. http://www.intel.com/technology/pciexpress/devnet/docs/WhatisPCIExpress.pdf
17. http://www.RapidIO.org
18. http://www.hypertransport.org
19. http://www.morethanip.com/products/posphy
20. http://www.atmforum.com/standards/approvedOct03.html
21. http://www.amcc.com/Compinfo/PressReleases/xilinx4_01.htm
22. http://www.10gea.org

23. http://hsi.web.cern.ch/HSI/fcs/spec/overview.htm
24. http://www.npforum.org/csixL1.pdf
25. http://www.techfest.com/networking/wan/sonet.htm
26. http://www.infinibandta.org/ibta

6 APPENDICES

A 8B/10B CODING

The 8b/10b coding was introduced in 1982 by A.X.Widmer and P.A.Franaszek [11] from IBM. This way of coding is used today in transmission protocols – synchronous, like Fibre Channel, and asynchronous, like Gigabit Ethernet. Its common usage stems from the following positive features:

- coding is binary,
- efficiency is close to the ultimate limit for 8b/10b codes,
- enables error detection,
- provides fast, synchronous clock synchronization with signal frequency (clock recovery),
- increases the extinction ratio,
- differentiates control bytes and data bytes,
- coding algorithm minimizes number of bit changes in coder,
- separation of coding to two parts (3b/4b i 5b/6b) simplifies coding algorithm,
- coding algorithm minimizes DC constant from transmission signal,
- hardware construction of transmitters and receivers is simple in realization.

A.I Coding algorithm

The 8b/10b coding relies on conversion od 8 input bits to 10 output bits send via any transmission channel. In order to improve the coding algorithm, the input bits are divided to two separate sub-groups: 5-bit and 3-bit. The bits and groups are signed as *ABCD* and *FGH*. Each of the groups is coded separately with the algorithm 5b/6b and 3b/4b. These processes convert the input bits to *abcd* and *fgh* and add one additional bit i and j to each group. These groups are joined together to form a single 10-bit output word.

The way of coding depends on the value of binary *disparity* signal. The *disparity* signal is zero or unity depending on the number of zeros and units in the previously sent 10-bit output word. For example, if the number of zeros is bigger than units, the value of *disparity* is changed to the opposite.

The 8b/10b coding assures the separation of data bytes from control bytes. When the control bytes are transmitted, the state of the *control* signal at the input of the coder is high. The method of coding is changed in this case. The coder is able to distinguish the kind of received byte.

A.II Decoding algorithm

The decoder converts 10 bits back to 8 bits of the input data. Similarly as in the coder, here the bits re divided to two parts: 6-bit and 4-bit. Next, the decoding processes restore 5-bit and 3-bit of original parts. They are combined to the output 8-bit word. The decoder recognizes the type of control byte by investigation of particular bits of the received word. The control word is signalized by the setting of the *control* line to the high state.

Error discovery in the sent words is done on the level of 6-bit and 4-bit parts as well as on the level of the whole word. The checking embraces the investigation of conformance with allowed sequences of coding. When an erroneous word is received, which fulfills the

condition of the control word, but could not have been sent from the coder, the transmission error signal is also reported. The discovery of error in the *disparity* signal is done nondependently for the 6-bit group and 4-bit group. The groups are recovered and compared to the expected values. When the error is discovered in the *disparity* signal in a group, a general error is reported of the *disparity* signal and the error concerning this signal in each group separately.

B   SERIAL TRANSMISSION TECHNOLOGIES IN FPGA

The SERDES (serializer/deserializer) circuits realize data serialization from several parallel inputs to a single serial output. The aim is to transmit data via a narrow and fast transmission channel. At the output end of the channel a reverse operation is performed. The original parallel form of data is recovered at the receiving end of the transmission system with serdes chips. The serdes chips may additionally code and decode data, do correction, synchronization, etc.

There is available a number of simple and specialized serdes chips on the market. Some of them are standalone chips like TLK2501 by TI, some are inbuilt in the FPGA matrices by Altera and Xilinx. Comparison of some properties of these circuits were gathered in table 4.

Chosen parameters	block TLK2501 from Cyclone EP1C20 (Altera)	Family Virtex II Xilinx	Family Stratix GX Altera
Name		Rocket I/O	Serial Light
Serializer / deserializer	+	+	+
Coding and decoding 8b/10b	+	+	+
Data rate of transceivera	1.5 – 2.5 Gbit/s	**622Mbit/s - 3.125 Gbit/s**	**400Mbit/s - 3.125 Gbit/s**
Number of channels	1	**20**	**20**
Aggregated transmission	1.5 – 2.5 Gbit/s	*do 63.5 Gbit/s (Full-Duplex)*	*do 63.5 Gbit/s (Full-Duplex)*
Maximal length of word	20 bit	**32 bit**	10 bit
Clock frequency	75 – 125 MHz	50 – 156.25 MHz	**20 - 650 MHz**
Rise/fall time	1 ns	120 ps	60-130 ps
Latency in the transmitter	**2.125 - 2.375 clock period**	8 - 17 clock period	3 - 8 clock period
Latency in the receiver	**4.75 - 6.6875 clock period**	25 - 42 clock period	7 – 32 clock period
Total latency	**7 - 9 clock period**	33 – 59 clock period	10 – 40 clock period
Power supply	1.7-3.6 V, 0.8 V / 1.5V, 1.8V, 2.5V, 3.3V	2.5V, 3.3V	1.5V, 1.8V, 2.5V, 3.3V
Power consumption [1]	**360 + 120 mW**	920-1100 mW	**450 mW**
Serviced interfaces and protocols	10/100 oraz Gigabit Ethernet, POS-PHY L2 i L3 UTOPIA L2 i L3	10 Gigabit Ethernet XAUI, Gigabit Ethernet, Fibre Channel, SONET/SDH, InfiniBand, RapidIO, HyperTransport, POS-PHY L3 i L4, Flexbus 4, XGMII, CSIX-L1, PCI, PCI Express	10 Gigabit Ethernet XAUI, Gigabit Ethernet, Fibre Channel, SONET/SDH, InfiniBand, Serial RapidIO, HyperTransport, POS-PHY L4, NPSI(CSIX-L1), PCI Express, SMPTE 292M

(1) for 4-channel transceiver

Tab. 4   Comparison of parameters of chips TLK2501 TI and Cyclone EP1C20 (Altera), with FPGA chips Virtex II Xilinx and Stratix GX Altera

The applied solution, in the presented hardware, of connection of the TLK2501 circuit with Cyclone FPGA introduces considerably lower latency, for lower data rates, in comparison with the serdes chips integrated inside the FPGA. The costs of such realizations are lower. The newest versions of FPGA chips should be, therefore, used for the highest required data rates and much bigger number of channels. The chip families Stratix GX and Virtex II possess comparable transmission parameters and the number of available channels. The most important differences are in the served interfaces and protocols, what was characterized in the further part of this chapter.

The interfaces served by FPGA chips, mentioned in table 4 (Cyclone, Virtex-II and Stratix-GX) embrace data transmission at various levels of the OSI model and concern different devices. They create four groups of interfaces:

- Parallel synchronous systems (standards): PCI 32/33, PCI 64/66 and PCI Express,
- Parallel synchronous sources: RapidIO, HyperTransport, POS-PHY L3 & L4, Flexbus 4, XGMII and NPSI (including in this CSIX-L1),
- Fast serial interfaces, realizing particular transmission protocols: Gigabit Ethernet, 10 Gb Ethernet (XAUI), Fibre Channel, SONET and Infiniband,
- Advanced memory interfaces: ZBT SSRAM, DDR SDRAM and QDR SSRAM.

Table 5 presents a comparison of protocols of data transmission with the rate of 10 Gbit/s.

Name of interface	Size of the biggest frame [B]	The biggest length of frame [B]	Amount of sent data for data rate 10 Gbit/s [b/s]	Amount of sent data after 8b/10b coding for data rate 10 Gbit/s [b/s]
10 Gigabit Ethernet	1500	1526	9,829,619	7,863,696
CSIX-L1	256	260 (264*)	9,846,154 (9,696,970*)	7,876,923 (7,757,576*)
HyperTransport	64	72 (80*)	8,888,889 (8,000,000*)	n/a**
InfiniBand	4000	4040	9,900,990	7,920,792
PCI Express	4096	4116 (4120*)	9,951,409 (9,941,748*)	7,961,127 (7,953,398*)
RapidIO	256	293	8,737,201	6,989,761
SDH/SONET	150,336	155,520	9,666,667	7,733,333
UTOPIA 4	48	52	9,230,769	7,384,615

*optionally with the usage of additional redundant bits

** Due to its construction, the HyperTransport does not require 8b/10b coding 8b/10b [14]. Thus, it is characterized by large amount of data sent in packets.

Caution: version of Fibre Channel protocol of data rate 10 Gbit/s is not serviced by the described devices, thus, was not placed in the table

Tab. 5.   Comparison of interfaces inbuilt in the FPGA chips against the relative amount of data transmitted at the constant data rate of 10 Gbit/s

It is to be noted, that the data included in table 5 are very close to each other. All the presented interfaces are characterized by high efficiency.

The currently available commercially transceivers on the market have data rates up to 40 Gbit/s. That is why the manufacturers of FPGA chips try to increase the internal and I/O data rates. The Virtex IV chip, released by Xilinx in September 2004, works at the maximum rate of 11.1Gbit/s via one of the 8 (maximally up to 24) channels. The channel can work with the word width from 32-bit up to 40-bit. Additionally the chip possesses inbuilt 8b/10b and 64b/66b coding/decoding

Next part of the chapter characterizes in short the most important interfaces of serial transmission available in the new families of FPGA chips. The description includes, in particular, the fastest interfaces dedicated to cooperate directly with optical transceivers and optical fibers.

B.I   PCI Express

PCI Express [13] replaces the PCI standard which has confined transmission rate to 132 MB/s for the shared bus. The *PCI Express* has each pin connected to a separate duplex line creating point-to-point transmission channel. The lines can be additionally connected in series. The current available data rates are at the level of 250MB/s for each line (i.e. 7.8 GB/s in each direction, with 32 lines).

B.II   RapidIO i Serial RapidIO

The RapidIO [17] is a standard replacing transmission realized by the PCI bus. The place of a shared bus is exchanged by point-to-point transmission. The devices may communicate directly, without the usage of host controllers or bridges.

The RapidIO is a protocol, which uses direct addressing (direct or identification). The transmission bases on the routing tables in the switches. Changes in the transmission routes for data is fast and efficient. This transport (like HyperTransport) is more transparent than in the case of InfiniBand technology. The standard may cooperate with existing software solutions.

The Serial RapidIO [17] protocol is an extension of RapidIO of a new physical layer. It enables transmission with data rates of 1.25, 2.5 and 3.125 Gbit/s in both directions between devices. The transmission is done via switches without any need to use additional functions.

B.III   HyperTransport

The *HyperTransport* [18] bus realizes fast duplex transmission between processors and I/O devices. It replaces the extended buses like PCI. It has point-to-point links and the data width may be 2, 4, 8, 16 or 32 bit with the rate of 22,4 GB/s. It has not only very broad transmission bandwidth but also low latency and good scalability (from 200MHz to 1.4 GHz), low power consumption, transparency to PCI software and low crosstalk. It is compatible with *PCI*, *PCI-X* and *PCI-Express*. HT enables easy hardware implementation of connections realized in the LVDS (Low Voltage Differential Signaling) standard.

B.IV   POS-PHY L3 i L4

The interface *POS-PHY L3* (Packet Over Sonet Level 3) [19] realizes connections between physical layer (frames of *SDH / SONET* or *Gigabit Ethernet*), and devices of data link layer (transferring devices *ATM, Gigabit Ethernet*) with the rate up to 3.2 Gbit/s for the words of 8 or 32 bit in width. The interface *POS-PHY 3* works with the clock rate not bigger than 104 MHz. The interface is used in switches and IP routers and in the devices managing the network traffic. It enables the effective change of transmitted data in different formats (different transmission data rates and data bus width).

The *POS-PHY L4* [19] is an interface which extends the possibilities of the POS-PHY L3. The transmission rate is increased here up to 10 Gbit/s. It is possible to service the devices working in *STM-64* standard.

B.V   UTOPIA

The *UTOPIA* [20] interface (Universal Test and Operations PHY Interface to Asynchronous Transfer Mode) realizes the communication between physical layer and the modules form upper layers, like the layer of ATM link. The interface of physical layer takes

into account the transmission properties of the used medium. The transmission is realized by the LVDS bus. There are now three versions of the interface determining the width of the word and transmission rate:

- *UTOPIA Level 2* uses 8-bit and 16-bit word for clock signal of the frequency not bigger than 50 MHz. The biggest reached rate is 622 Mbit/s.

- *UTOPIA Level 3* provides transmission data rate which depends on the word length, and respectively for word lengths 8-, 16- i 32- bit, is equal to 800 Mbit/s, 1.6 Gbit/s and 3.2 Gbit/s. The biggest clock frequency for this realization of interface is 104 MHz.

- *UTOPIA Level 4* for word lengths 8-, 16- and 32- bit realizes the data rates 2.5, 5 and 10 Gbit/s. The maximum clock frequency is 415 MHz.

B.VI   Flexbus 4

The *Flexbus 4* [21] is an interface which enables the routers *packet-over-SONET/SDH (POS)* to send the native IP packets directly in the frames of *SONET/SDH*. The transmission with the rate 10 Gbit/s is possible between the processor of data link layer and a frame circuit of physical layer. The *Fexbus 4* interface sends 64 data bits during a single clock period. It is also possible to use 16-bit word for transmission data rate of 2,5 Gbit/s.

B.VII   CSIX-L1

The interface *CSIX-L1* (Common Switch Interface Layer 1) [24] enables transmission on the physical layer between the network processor (in particular of Traffic Manager type – i.e. a device which manages the paths of virtual memory and data) and a switching fabric. The interface *CSIX-L1* was designed for short connections, up to 20 cm. It provides transmission data rate up to 32 Gbit/s. It may cooperate with protocols managing the rates 10Gbps and bigger. These protocols may base on continuous flow of cells (ATM) and packet transmission (SDH/SONET).

B.VIII   SDH i SONET

The *SONET* (Synchronous Optical NETwork) and *SDH* (Synchronous Digital Hierarchy) are standards for synchronous trunk transmission [25]. They were originally prepared for telephony applications. They use TDM (time domain multiplexing). They realize network control and transmission quality monitoring, what is necessary in trunk networks. The data rates are 10 Gbit/s (*OC-192* for *SONET* and *STM-64* for *SDH*). The *SDH* networks may have loop and mesh architecture. The mesh architecture requires more complex network management system.

B.IX   10 Gigabit Ethernet

The *10 Gigabit Ethernet* [22] is a next hierarchical step in the development of the *Ethernet* protocol. The Ethernet is commonly used in *LANs* (Local Area Network) and *MANs* (Metropolitan Area Network) [16]. The introduction of IEEE 802.3ae standard for *10 GbE* opened its wide applications in *WAN*. The protocol bases on multi-access algorithm with detection of collisions *CSMA/CD* (Carrier Sense Multiply Access with Collision Detection). The difference with previous versions of Ethernet is increasing the nominal length of the frame up to 512 bytes. The algorithm *CSMA/CD* was additionally extended with *Packet Bursting* function, which provides management of packet stream control. When the packets have small lengths they may be transmitted in groups. Framing small packets increases transmission efficiency of the Ethernet channel. The *10 Gigabit Ethernet* protocol uses only full-duplex transmission. This communication is predicted mainly for optical fibre links – multimode and singlemode. The data are sent in three transmission windows of commercial fibers. The data rates may be made compatible with *STM-48* and *OC-192*.

B.X   XAUI

The *XAUI* [22] interface (10 Gigabit Attachment Unit Interface) was designed to simplify the implementation of 10Gbps transmission module in integrated circuits. It bases on the *Gigabit Ethernet* interface with 8b/10b coding. It provides channel transmission with the rate 2,5 Gbit/s. It is possible to parallelize four such channels to provide 10Gbps. Now the *XAUI* interface is one of the most popular solutions in TX-RX circuits using the aggregated data rate of 10 Gbit/s.

B.XI   Fibre Chanel

The *Fibre Channel* [23] is a protocol commonly used in networks using mass memories, like *SAN* (Storage Area Network). It enables transmission between processors themselves, as well as between processors and peripherial devices. It can work in loop and fabric architectures. It realizes also channel transmission (point-to-point). The *Fibre Channel* is a synchronous protocol. The data rate reaches 10Gbps for the bandwidth only a little bigger than for *10Gbit Ethernet*. The length of transmission hop depends on data rate and the physical medium.

B.XII   InfiniBand

The *InfiniBand* [26] protocol was designed for data transmission for big cluster like computer systems. It bases on very fast network switches, which control the transmission between sub-networks. It can connect thousands of processors. The maximum data rates are of the order of 10Gbpsbut are planned for 120 Gbps. The link length of the *InfiniBand* is local only and reaches up to 10 m for copper cable and several hundred m for fiber cable.