

# Vector Modulator Card for MTCA-based LLRF Control System for Linear Accelerators

Igor Rutkowski, Krzysztof Czuba, Dariusz Makowski, *Member, IEEE*, Aleksander Mielczarek, Holger Schlarb and Frank Ludwig

**Abstract**—Modern Low Level Radio Frequency (LLRF) control systems of linear accelerators are designed to achieve extremely precise field amplitude and phase regulation inside superconducting cavities. One of the crucial components of the feedback loop is a vector modulator used to drive the high power RF chain supplying accelerating cavities. The LLRF control systems for the Free Electron Laser in Hamburg (FLASH) and European X-ray Free Electron Laser (XFEL) are based on emerging Micro-Telecommunications Computing Architecture (MTCA,  $\mu$ TCA) platform offering numerous advantages for high performance control systems.

This paper describes the concept, design and performance evaluation of world's first Vector Modulator (uVM) module dedicated for LLRF systems compatible with MTCA specification. The module has been designed as a double-width, mid-size AMC form factor Rear Transition Module (RTM) according to developed by PCI Industrial Computer Manufacturers Group (PICMG), MTCA.4 specification.

The uVM board incorporates digital, analog and diagnostic subsystems. The digital part is based on Xilinx Spartan 6 family FPGA, with several fast gigalink connections to control module. The uVM module is equipped with an Intelligent Platform Management Interface (IPMI) circuit required by MTCA.4 standard. The FPGA controls the analog part, which includes fast, high-precision DACs, IQ modulator chips, programmable attenuators, power amplifier and fast RF gates for external interlock system. The RF chain can be adopted to different carrier frequencies covering frequency range from 50 MHz to 6 GHz. The design has been carefully optimized for high linearity and low output signal phase noise. The diagnostic system of RF chain allows to monitor input and output power levels and detect failure in RF part. Low noise and high performance clocking system makes the uVM an universal device for applications exceeding the LLRF control system. Extensive tests of the board were performed and measurement results are presented and discussed in this paper.

**Index Terms**—Low Level Radio Frequency, Vector Modulator, xTCA, Micro-Telecommunications Computing Architecture, Rear Transition Module

## I. INTRODUCTION

THE modern superconducting linear accelerator facilities, such as the European XFEL, use precisely controlled RF field for electron beam acceleration [1]. The field parameter control is performed by a Low Level Radio Frequency (LLRF) control system [2]–[5] which should assure up to 0.01 % of amplitude and 0.01° of phase regulation accuracy while

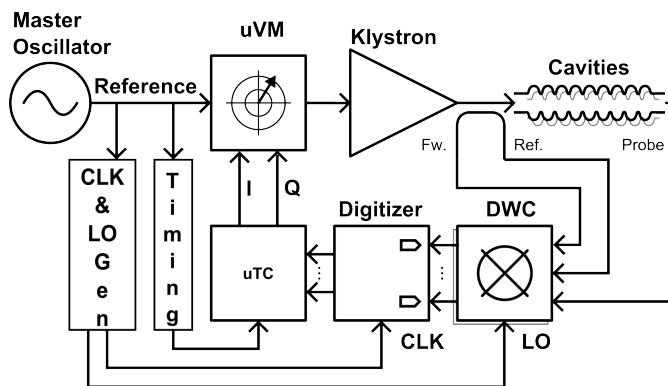


Fig. 1. The LLRF system architecture

parallel processing of almost 100 Radio Frequency (RF) signals from cavities. Such requirements make then design of the LLRF a very challenging task that requires using state-of-the-art technology.

Requirements given above together with obligatory high operational availability force the LLRF system designers to build a compact hardware including both powerful digital processing units with Gb/s data transmission, low-latency links and high precision RF and analog circuits. Commonly used hardware standards like VME or PXI [6] exhibit serious limitations for such systems as the new LLRF (for example too slow backplane communication, no hot swap, lack of a hardware management). Therefore new telecommunication hardware standard (Micro-Telecommunications Computing Architecture - MTCA) was adopted to physics experiments requirements [7] and has been selected as a hardware platform for the Free Electron Laser in Hamburg (FLASH) and European X-ray Free Electron Laser (XFEL) control systems. The MTCA standard offers modularity, scalability, maintainability and remote diagnostics capabilities [8] – crucial features for large scientific machines.

The simplified block diagram reflecting the LLRF system architecture and physical realization in MTCA system of XFEL is shown in Fig. 1. The electromagnetic field used for electron beam acceleration is stabilized in superconducting cavities operating at resonant frequency of 1.3 GHz or 3.9 GHz. High-frequency input and output signals of accelerating cavities are converted down to an Intermediate Frequency (IF) by multichannel downconverter modules (DWC) designed as Rear Transition Module (RTM) cards. IF signals are analog-to-digital converted by an AMC digitizer module. Data from

Manuscript received June xx,2012

I. Rutkowski and K.Czuba are with Warsaw University of Technology (WUT).

D. Makowski and A. Mielczarek are with Technical University of Lodz (TUL).

H. Schlarb and F. Ludwig are with Deutsches Elektronen-Synchrotron (DESY).

up to eight digitizer modules is collected by the main LLRF MTCA controller module (uTC realized as AMC card [9]) with the use of Low-Latency Links (LLs) available on the MTCA AMC backplane [10]. The uTC uses the acquired data to calculate the output signal that is used to drive an RTM Vector Modulator card. The digital data sent by the uTC is deserialized and digital-to-analog converted by fast digital-to-analog converters (DACs) at the uVM card in order to drive I and Q inputs of a modulator chip. The LLRF system feedback loop is closed by a klystron supplying accelerating cavities. The performance of the Vector Modulator is therefore one of factors limiting performance of the entire LLRF system and also its reliability together with accelerator operation safety. Therefore the uVM design must incorporate state-of-the-art technology, include on-board diagnostics and support high-availability solutions.

The uTC AMC board interface directly the uVM card by the Zone 3 connectors with a low-latency gigabit link. This is an unique feature of the MTCA.4 standard allowing interfacing physically separated high performance analog and digital modules in a modular, hot-swappable and fully managed system.

The uVM card has been designed to fulfill stringent requirements of the FLASH and XFEL control systems and to provide additionally diagnostic and interlock functionality in a very compact RTM format [7]. For systems requiring lower computational power and less channels the uVM can interface directly the digitizer card over the Zone 3 connectors in order to create a cheap control system. The uVM card also supports the MTCA RF Backplane (uRFB [11]) allowing for reduction of RF cable connections and supporting maintainability of the entire system.

According to authors best knowledge the card presented in this paper is the first publicly known implementation of vector modulator module compatible with the MTCA.4 RTM specification.

## II. REQUIREMENTS FOR VECTOR MODULATOR

### A. General requirements

The Vector Modulator card should allow two modes of operation:

- standalone mode - without the main controller module,
- system (cooperation) mode - connected to the uTC or MTCA digitizer module such as Struck SIS8300<sup>1</sup>.

The standalone mode is suitable for debugging, quality control and measurements of the uVM board. During normal LLRF operation the cooperation mode is used.

### B. Functional requirements

The vector modulator board should fulfill the following requirements concerning the MTCA.4 standard:

- double-width, mid-size AMC form factor RTM [7]
- hot-plug switch and LEDs required by Intelligent Platform Management Interface (IPMI) standard [12] on the front panel

- management and diagnostics according to IPMI standard

Integration with LLRF system is assured by:

- data links between the controller and the VM. Minimum 10 bidirectional, differential pairs are required.
- compatibility with uRFB.

In the cooperation mode, the uTC serializes and sends calculated IQ drive signals to the vector modulator card through the Zone 3 connector using a gigabit link [13]. The uVM card is responsible for performing a single sideband modulation with a deserialized modulating signal in two independent but identical channels. In LLRF system the first channel is used for driving the klystron and the second for system calibration.

DACs generate baseband analog signals driving the quadrature modulator chips. Those chips are fed with a low phase noise RF reference signal.

Input and output signals' power should be monitored (in digitized format) for failure detection. The output signals can be turned off in emergency situations with a low latency RF switch called RF gate. SMA connectors for input and output signals should be mounted on the front-panel.

Clocks for the converters and the FPGA can be synthesized on-board using the RF input signal as a reference or provided externally over the RF backplane or front panel SMA connector.

Differential signaling standards are preferred for all types of signals because of their better noise immunity and resistance to electromagnetic interference compared to single-ended signaling.

### C. Electrical requirements

Each channel should provide signal with maximum power level of +10 dBm or more, attenuated in the range of -15 dB to 0 dB with 5 bit resolution (while maintaining full I and Q resolution) controlled by the software. Desired RF channels' crosstalk should be -70 dB or better.

The baseband IQ signals should be low-pass filtered of 50 MHz before entering modulator chip input.

Besides the main payload power supply (+12 V) provided according to the MTCA standard, +7 V and -7 V rails dedicated for analog RF circuits are provided by uRFB.

### D. Requirements for European XFEL

The European XFEL requires extremely stable amplitude (0.01%) and phase (0.01°) regulation of accelerating field in order to provide a bunch arrival time jitter of less than 60 fs (all values RMS). Detailed analysis of phase noise budget for LLRF system can be found in [14]. Phase noise above the control loop bandwidth is filtered by the cavity (which can be modeled as first order low pass with the cutoff frequency of 200 Hz). Therefore effort should be made to reduce distortions and noise at low frequencies.

In order to achieve the desired field amplitude and phase stability following electrical requirements have been put

- non-linearity on IQ Plane  $\leq 0.1\%$
- short-term noise  $\leq -160$  dBc/Hz

<sup>1</sup><http://www.struck.de/sis8300.html>

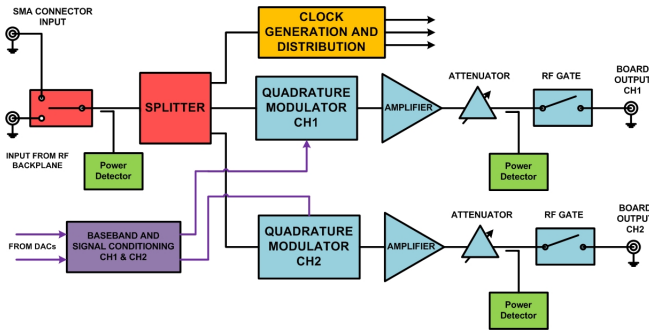


Fig. 2. Block diagram of the analog subsystem of the Vector Modulator card.

### III. DESIGN DESCRIPTION

#### A. Previous designs

According to authors knowledge there is very limited list of references describing similar designs.

Instrumentation Technologies<sup>2</sup> has designed an AMC vector modulator card [15] combining the functionality of the vector modulator and the controller cards, but performance evaluation of the RF modulation chain has not been published.

Realization of a vector modulator board working in ATCA based LLRF system has been described in [16]. That device is full size AMC module composed of two PCBs connected using a 120 pin high speed connector. It occupies two parallel slots and has only one RF channel. Results of the tests have not been included in the paper.

No data is available for direct comparison, but taking into account the performance of quadrature modulator chips offered by leading semiconductor manufacturers (Hittite, Analog Devices, Texas Instruments) meeting the requirements given in II-D present a significant challenge for the designers and the module described in this paper reaches performance limits of current technology.

#### B. Analog Subsystem

Key components of the analog part of the uVM board have been identified by requirements described in subsection II-B. Based on given functional and electrical requirements a structure of analog subsystem has been proposed.

The block diagram of the vector modulator board's analog part is presented in Fig. 2. The RF switch selects the input signal either from SMA frontplate connector or from the uRFB. The switch is controlled digitally by the FPGA and therefore the signal source can be selected on-line by the system control software. The power splitter distributes the RF Reference signal to two independent modulator channels as well as to the clock generation and distribution circuit. Each RF chain is composed of an IQ modulator, an amplifier, a programmable attenuator and an output gate. Three power detectors monitor input and output signal power. Detailed considerations on each block will be provided in the text below.

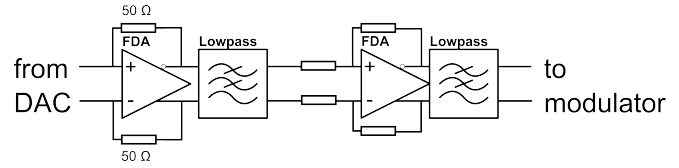


Fig. 3. Block diagram of the baseband signal conditioning chain.

1) *RF chain*: The principle of the operation of an integrated quadrature modulator has been described in [17], including linear and nonlinear errors. It simultaneously controls amplitude and phase of the output RF signal. Such chips are widely used in wireless communication because they can be used to realize any digital modulation scheme.

Signal modulation chains should be optimized for achieving low noise floor, low linear and nonlinear distortions as well as coupling of external signals for optimal LLRF system performance.

The most important element of each RF channel is quadrature modulator. The parameters of the modulator have the most significant impact on the chain performance. Low noise, wide band, high linearity integrated circuit with matched input and output impedances has been used.

Output signal's nonlinearity can be considered in the aspect of nonlinear signal driving the modulator and odd orders intermodulation distortions. Linearity of the modulating IQ signal is determined by the performance of selected DACs and designed signal conditioning circuit. Intermodulation distortions have been minimized by choosing optimum operation point of the modulator chip and amplifier. Harmonics level of the carrier signal at the output and their modulation have been considered unimportant to this project.

The modulator chip which is the first element of each RF channel determines the noise floor achievable for the entire chain. Signal to noise ratio is slightly (0.5 dB) deteriorated by following elements of the chain.

Longer traces of RF signals should be completely hidden within inner layers to minimize the pick up of external interference and noise.

To meet the desired power level a low noise, linear RF amplifier delivering a power of +15 dBm has been used. Such level has been selected to assure maximum power level of +10 dBm at the board output.

The attenuator can provide attenuation in range of 0 dB to 15.75 dB, digitally controlled in 0.25 dB steps.

Logarithmic power detector with 70 dB dynamic range, high linearity (1 dB error over 60 dB range) converts input RF signal to a proportional DC voltage. This signal is low-pass filtered (with corner frequency of 48 Hz) and amplified in order to use full scale of a analog to digital converter.

Compatibility with uRFB is provided by two connectors - one multi-coaxial (RF reference input) and one multi-differential pairs (analog power supply and clock).

2) *Baseband chain*: High resolution (16 bit), fast (160 MSPS) DACs generate baseband differential analog IQ signals.

Selected DAC chips have two independent, complementary current-source outputs each with full scale current set by external resistor and software. Such outputs achieve best linearity

<sup>2</sup><http://www.i-tech.si/>

when working in constant voltage mode. The compliance range of the DAC and the common mode of the modulator chip do not allow to interface them directly.

Therefore two stage baseband signal conditioning circuit has been designed (block diagram visible in Fig. 3). First stage performs complementary current-to-voltage conversion (preserving constant voltage at the DAC output) and low-pass filtering, while the second amplifies the signal, filters it and changes it's common mode (set by another DAC). The imbalance of the whole baseband chain and inputs of the modulator can be calibrated using software capabilities of the main DAC to control amplitude and offset on each channel.

3) *Clocking*: Another factor influencing the modulated signal's quality is the spectral purity of the signal clocking DACs. Therefore high performance clock generation and distribution components have been used. Clock can be generated by frequency division of the RF reference signal or distributed directly by specialized 10-output chip (6 LVPECL and 4 LVDS).

4) *Power supply*: Digital circuits can be powered directly by single stage DC/DC converters. The analog part requires two stage supply with additional low-dropout, low-noise analog regulators and suitable passive filtering.

Improved RF quality substrate material has been chosen as a compromise between price and performance.

### C. Digital Subsystem

The digital subsystem of the uVM module is composed of the Spartan 6 FPGA device, power supply unit and IPMI management circuitry required by MTCA.4 specification. The block diagram of the digital part is presented in Fig. 4. The uVM FPGA controls main DACs, clock distribution circuit, attenuators, RF power monitoring circuit, monitoring ADC and base-band DAC. The device can be controlled using diagnostic USB interface available on the uVM face-plate when operating in stand alone mode.

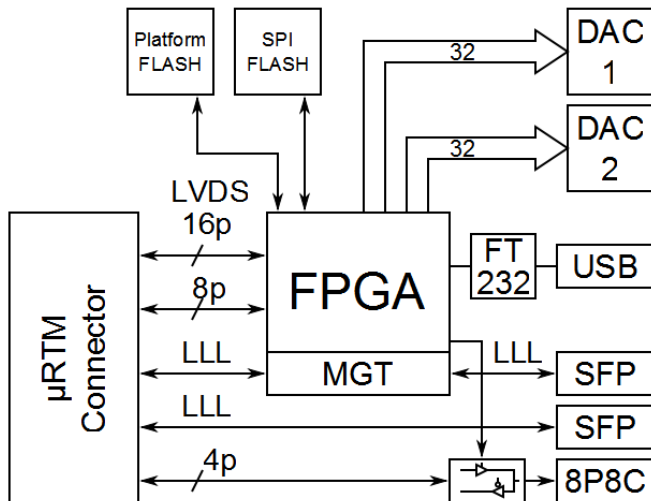


Fig. 4. Block diagram of the digital subsystem of uVM

The uVM module communicates with uTC board in the cooperation mode using digital signals only. The zone 3

connector provides two low-latency serial connections and parallel, general purpose LVDS signals, see Fig. 4. One of the low-latency serial connection is used as a main data transmission channel between uVM and uTC. The second high-speed serial link is provided between the uTC FPGA and the SFP (Small Form factor Pluggable) transceiver available on the uVM face-plate. This LLL connection can be used for connecting other LLRF subsystems. In addition, four 8P8C modular jack LVDS (Low-Voltage Differential Signaling) signals are available on the uVM face-plate. These signals can be used to connect additional subsystems of the LLRF control system, e.g. Lorentz Force Detuning compensation module.

The LVDS signals available on the zone 3 connector can be used for control and data transmission when the uVM module is connected to SIS8300 digitizer board. The LVDS signals are used for FPGA in system programming and FPGA PROM firmware upgrade [18].

1) *Module Management*: The MTCA.4 standard requires management system for RTM management and diagnostics. The subsystem is used for module activation, deactivation during hot-plug procedure, temperature and voltages monitoring. It provides also FRU (Field Replaceable Unit) hardware description according to IPMI standard [12].

The uVM board is equipped with basic management and hardware monitoring, as illustrated in Figure 5.

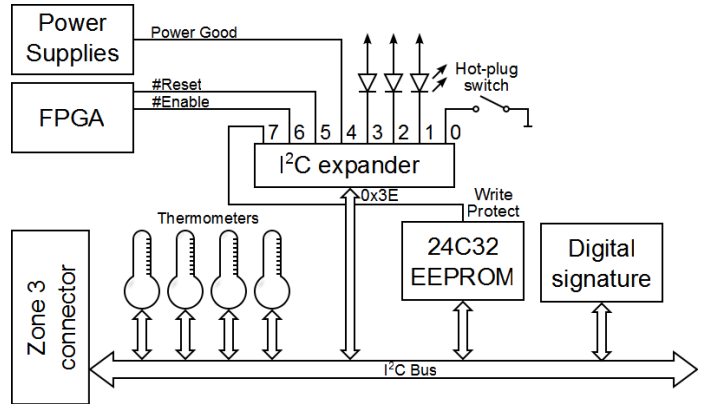


Fig. 5. Block diagram of the module management subsystem

The subsystem is based on 8-bit I<sup>2</sup>C expander. It is responsible for reading hot-swap sensor, driving optical indicators required by IPMI standard and monitoring power supply diagnostic signals. It also provides two-wire interface to the FPGA and controls the 'write protect' signal of the on-board serial EEPROM memory. The EEPROM is used to store FRU information describing RTM module capabilities according to IPMI and AMC standards. The board is equipped with four MAX6626 thermometer chips placed in the most critical parts of the uVM board. In addition, every uVM board has unique 64-bit digital signature.

## IV. TESTS

Extensive laboratory tests have been performed on the vector modulator card. First, the uVM module has been configured for operation in the standalone mode. The external computer

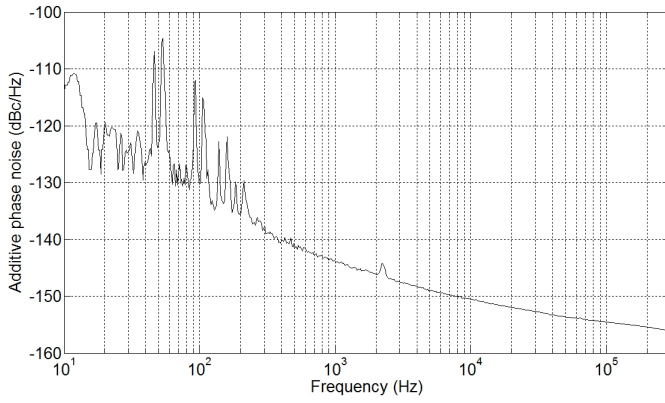


Fig. 6. Additive phase noise spectrum of the vector modulator card.

TABLE I  
INTEGRATED PHASE NOISE CONTRIBUTION PER DECADE

Frequency band (Hz)	Additive jitter (fs RMS)
10 - 100	1.7478
100 - 1k	0.7695
1k - 10k	0.4883
10k - 100k	0.8561
10 - 100k	2.6527

TABLE II  
SPECTRUM OF THE MODULATED SIGNAL

Harmonic	Ch 1 Power [dBm]	Chl 2 Power [dBm]
3	-50.77	-49.75
2	-49.66	-50.82
Wanted sideband	15.26	15.16
Carrier	-46.75	-58.52
Unwanted sideband	-33.48	-45.24
-2	-44.33	-46.87
-3	-16.43	-18.09

has been used for configuration of components of the uVM module.

#### A. Analog subsystem tests

The additive phase noise of the uVM board has been measured using Blue Phase 1000 [19] from Wenzel Associates with oscillator generating 1.3 GHz signal with very low noise floor (-180 dBc/Hz at 20 MHz offset) being the RF reference signal. I and Q signals have been set to constant, maximum values.

Spectrum of output signal has been presented in fig. 6. Strong peaks around frequency 50 Hz and its harmonics are visible, but the additive phase noise of the device is very low above 250 Hz. Total contribution per decade has been calculated and presented in Table I. Integrated phase jitter in band 10 Hz - 100 kHz (limited by test system corner frequency) is  $1.2415E-3^\circ$  ( $2.1668E-5$  rad). This result is 18 dB better than total budget for the phase stability of the entire system.

Calibration has been performed by manual tuning of offsets and gains on each baseband I and Q channel while realizing modulation of the input signal with complex sine wave, following a procedure described in [20]. Power levels of carrier, sidebands and their harmonics have been measured

and results are presented in Table II. Channel 2 linear errors (carrier leakage and unwanted sideband suppression) level meet the requirement presented in section II-D by a small margin and fidelity of the signal at channel 1 output is not sufficient.

#### B. Digital subsystem tests

The digital connections have been tested when the module has been installed in 12-slot Elma chassis [21] equipped with MCH designed by NAT [22] and AMC-1000 card by Adlink [23]. The uVM has been connected with uTC module (revision 1.3) [9]. The main FPGA of the uTC module sends data with CRC checksum using two LLL and all available LVDS channels. The FPGA available on the uVM module receives data and calculate CRC. When mismatch in CRC is detected a suitable error counter for tested link is incremented. The calculated BER (Bit Error Rate) for LLL working with 3.125 Gbps is better than  $2 \cdot 10^{-14}$  bit.

#### V. CONCLUSION

The first design of a MTCA.4 compatible vector modulator card is described in this paper. It is a 2-channel RTM module designed for operation in broad signal frequency range of between 50 MHz and 6 GHz. The designed module incorporates Spartan 6 FPGA used for fast communication with AMC modules and for driving 16-bit, 160MSPS DACs. Auxiliary features have been added like on-board programmable attenuators, RF-gate and monitoring circuits. Board has been physically split to analog and digital part and RF design techniques have been applied for optimization of modulator parameters.

Extensive tests described in the paper prove the high performance of designed board. All those features make the designed uVM module a very universal and powerful device not only for LLRF but also for other signal processing systems.

#### ACKNOWLEDGMENT

"The research leading to these results has received funding from the European Commission under the EuCARD FP7 Research Infrastructures grant agreement no. 227579."

"This work has been supported by the European Union in the framework of European Social Fund through the Warsaw University of Technology Development Programme."

#### REFERENCES

- [1] Massimo Altarelli, et al., *The European X-Ray Free-Electron Laser Technical design report*, 2007.
- [2] S.N. Simrock, *Low Level Radio Frequency Control System for the European XFEL*, Proceedings of the International Conference in Mixed Design of Integrated Circuits and Systems 2006.
- [3] M. Champion, et al., *The Spallation Neutron Source Accelerator Low Level RF Control System*, Proceedings of the 2003 Particle Accelerator Conference.
- [4] M. E. Angoletta, *Digital Low Level RF*, Proceedings of EPAC 2006, Edinburgh, Scotland.
- [5] D. Makowski, W. Koprek, T. Jeyski, A. Piotrowski, G. Jaboski, W. Jamuna, K. Czuba, P. Predki, S. Simrock, A. Napieralski, *Prototype Real-Time ATCA-Based LLRF Control System*, IEEE Transactions on Nuclear Science Volume 58 Issue 4, August 2011.
- [6] C. Puls, *PXI and VXI modular instrumentation in the new milenium*, AUTOTESTCON '99. IEEE Systems Readiness Technology Conference, 1999.

- [7] PICMG, *PICMG Specification MTCA.4 Revision 1.0*, August, 2011.
- [8] S.N. Simrock, et al., *Conceptual LLRF Design For The European XFEL*, Proceedings of LINAC 2006.
- [9] D. Makowski, et al., *uTCA-based Controller*, 18<sup>th</sup> Mixed Design of Integrated Circuits and Systems, MIXDES, Gliwice, 2011.
- [10] D. Makowski, G. Jablonski, P. Predki and A. Napieralski *Low Latency Data Transmission in LLRF Systems*, Proceedings of 2011 Particle Accelerator Conference, New York, U.S.A., April 2011.
- [11] K. Czuba, M. Hoffmann, F. Ludwig, H. Schlarb, *RF Backplane for MTCA.4 Based LLRF Control System*, submitted for publication in Conference Record of Real Time Conference 2012.
- [12] PICMG, *Intelligent Platform Management Interface Specification*, Feb., 2004.
- [13] J. Branlard, et al. *The European XFEL System*, Proceedings of IPAC 2012.
- [14] F. Ludwig, M. Hoffmann, H. Schlarb and S. Simrock *Phase Stability of the next generation RF Field Control For VUV- AND X-RAY Free Electron Laser*, Proceedings of EPAC 2006.
- [15] Instrumentation Technologies, *Libera LLRF Brochure*, 2011.
- [16] K. Czuba, S. Bou Habib and D. Sikora, *AMC Vector Modulator Card for the LLRF System*, Proceedings of the International Conference in Mixed Design of Integrated Circuits and Systems 2011.
- [17] National Semiconductor, *Operating and Evaluating Quadrature Modulators for Personal Communication Systems*, USA, 1995.
- [18] D. Makowski, G. Jablonski, P. Perek, P. Predki, A. Mielczarek and A. Napieralski *Firmware Upgrade in xTCA Systems*, Real-Time Conference, Berkeley, California, 2012 .
- [19] Wenzel Associates Inc., *Blue Phase 1000 Phase Noise Test System Operations Manual*, USA, May 2007.
- [20] Eamon Nash, *Analog Devices Application Note 1039 : Correcting Imperfections in IQ Modulators to Improve RF Signal Fidelity*, 2009.
- [21] ELMA, *12 Slot Crate - MicroTCA.4 Rev. 1.0*, February 2012.
- [22] N.A.T., *NAT-MCH Users Manual*, March 2010.
- [23] Adlink, *AMC-1000 Mid-Size AdvancedMC Processor Module*, February 2012.