FPGA - BASED CONTROL SYSTEM FOR PIEZOELECTRIC STACKS USED FOR SC CAVITY'S FAST TUNER

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Abstract

The TESLA nine-cell SC cavities need a fast tuning system, which will be able to adjust its shape during the pulse operation. The first attempts were focused on the compensation of the repetitive and periodic distortion. The algorithms were implemented in Matlab and allow compensating only the Lorentz force detuning. However, the previous solution was too slow to be able to compensate the microphonics. The paper presents recent development in this field. The previously worked out algorithms are implemented in the FPGA-based control system. The SIMCON board is used, which allows to perform parallel, deeply pipelined calculations. The new approach allows integrating the algorithm dedicated for cavity shape control with the LLRF system used for vector sum control. Moreover, the new algorithm for on-line detuning calculation which is based on the electromechanical model of the cavity is presented. The system is tested with Module Test Stand (MTS) at DESY with the high gradient cavities (up to 37 MV/m). Two type of active elements are investigated the NOLIAC's and PI's – both multilayer, low voltage piezostacks. The paper will present the first results from carried out measurements.

MOTIVATION

During the pulse operation the cavity shape is deformed by microphonics and Lorentz Forces (LF) [1]. The first phenomenon is unpredictable, stochastic and reasonable fast but the amplitude of the deformation is low – in the range of a few tens of Hz of detuning from main resonance frequency. In contrary, the second effect is repetitive, predictable and its amplitude depends on the square of accelerating field. The resonance shifts caused by LF is quite slow but the detuning might be even 1 kHz, whereas the cavity bandwidth is only 230 Hz. Thus an electromechanical system for cavity fast compensation is mandatory for high gradients operation. The commonly used active elements for such systems are piezoelectric stacks. In the TESLA design, in the ACC7 cryomodule the piezoelements from NOLIAC(SCMAS/S1/A/10/10/20 /200/42/6000) and PI(P-888.90 PIC255) are currently assembled for all 8 cavities. A digital control system was designed for proper driving of piezoelectric actuators.

CONTROL SYSTEM SPECIFICATION

The ontrol system consists of low-level radio frequency control board with Virtex II pro FPGA, power amplifier and down-amplifier as buffer (see Fig. 1). Fast ADC and DAC converters with sampling rate up to 80 MHz are used for driving and sensing piezoelectric stacks as well as cavity probes. The FPGA-device is responsible for cavity detuning computation using the information from forward power ($U_{forward}$, $\phi_{forward}$), probe (U_{probe}, ϕ_{probe}) signal and electromechanical model of the cavity [2]. The signals from cavity probes as well as signals from piezoelectric sensors are dedicated for calculation of reference error signal in control feedback using the following formula:

$$\Delta\omega = \frac{-1}{2\cdot\pi}\cdot\left(\frac{\partial\phi_{probe}}{\partial t} - 2\cdot\omega_{1/2}\cdot\frac{\left|U_{fowrard}\right|}{\left|U_{probe}\right|}\cdot\sin(\phi_{forward}-\phi_{probe})\right)$$

Moreover FPGA device takes control of driving the fast piezoelectric actuators. The Simcon3.1L board has 10 ADC input channels and 4 DAC output channels. Therefore it is possible to compensate only 2 cavities independently using pipeline methods. For the future purpose the signals from probes will be calculated using the separate control board. The information of RF field phase and amplitude will be obtained using fast RocketIO optical links.

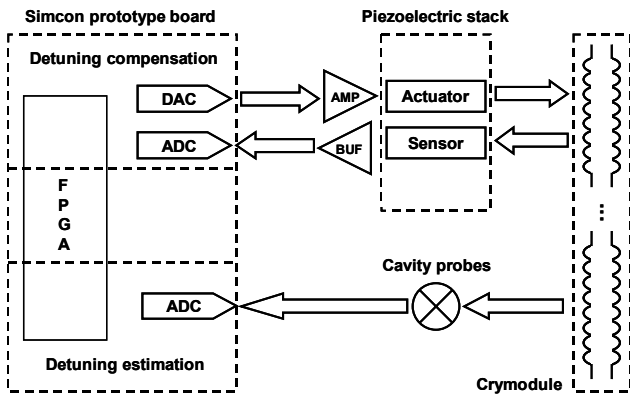

Figure 1: lock diagram of control system.

Digital Part Description

The system might be split into two main parts. The first module is dedicated for online detuning computation while the aim of the second one is an active detuning compensation using internal function generator. The project is designed in Virtex II pro FPGA. The main features for this architecture are:

- Internal block RAM modules
- Build-in 18x18 multipliers
- Integrated PowerPc processors and RocketIO

The width of multipliers was the main computation accuracy constraint. Therefore all computations are done using 18 bits 2'complement sign numbers. As it was

mentioned previously, the main goal for the digital part is the computation of a reference signal error between RF pulses and to estimate the fast piezoelectric actuator response to minimize cavity shape deformations.

Detuning Estimation Block

The computation algorithm is based on a electromechanical model of SC cavity [3, 4]. The raw data from the cavity probes are demodulated to I (in-phase) and Q (quadrature) components. The forward signal is initially calibrated to eliminate cross-talks between the forward and reflected power signals. The IQ signals are converted using Cartesian to polar conversion algorithms (square root, arcus tangent approximation). The output data are presented as the amplitude and the phase. The combinational division part of forward and probe amplitudes are performed using cascaded stages (radix 4). The phase difference between forward and probe signals are interpolated to compute sine value. The look-up table method has been used for this approximation purposes. An additional multiplier is used to calculate the final detuning signal. The most critical component for the design is the derivative filter block, based on FIR (Finite Impulse Response) principle. It is used for the linearization of the signal of the probe phase. The 32 taps filter is used which consumes 32 multipliers for the multiply and accumulate stages. Finally the multipliers have been replaced with 16 taps which repeat input samples (multiply by 1) and 16 taps which negate the input samples (multiply by -1).

Detuning Compensation Block

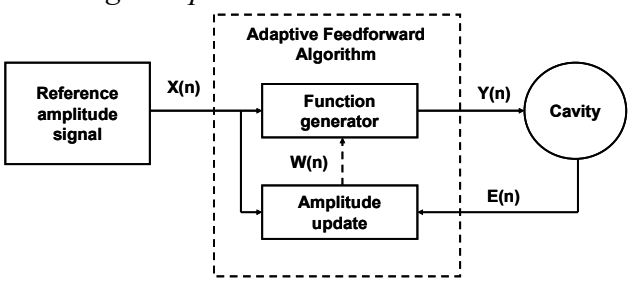

Figure 2: The Adaptive feed forward algorithm block diagram.

This module is used to apply to the system the method based on the adaptive feed forward algorithm (see Fig. 2). The initial setup for amplitude of driving signal is taken from internal memory block. The algorithm is focused on the online amplitude correction of the signal applied to the piezoelectric actuator. The correction error is estimated from the detuning computation block. Previously performed tests indicate that, when close to the optimal compensation settings, the amplitude of piezostack signal could be treated as a linear function of the RF gradient. As a result, the fast amplitude correction can be achieved for fine-tuning the system. The main block of the compensation system is an internal Function Generator build from internal RAM memory blocks. Only a quarter of sine wave values are initially stored in the memory. The full sine wave period is reconstructed using additional comparators and registers.

FIRST MEASUREMENTS AND RESULTS

Several tests of implemented control system were carried out in MTS at DESY. All 8 cavities in ACC 6 module with 16 assembled active elements were investigated. The main goal for the measurements was to discover parameters of the signal applied to piezostack (shape, amplitude, width and delay between the RF pulse, etc) for each cavity. The best results were achieved using half-sine pulse with a width of 5 ms (200 Hz) which roughly corresponds to the first mechanical resonance frequency of the tested cavities. Two methods of delay investigation were tested. The first one takes advantage of the cavity oscillation driven by the piezostack pulse, therefore it is based on a short time advance of the applied signal if compared to the RF pulse. The time value was set to 640 μs which corresponds to mechanical propagation time from piezostack to cavity. The second method is focused on second free oscillation induced by the piezo pulse (longer time advance around 4 ms). All the cavities mounted in the ACC6 module were tested with the highest possible operating gradients (see Fig. 3).

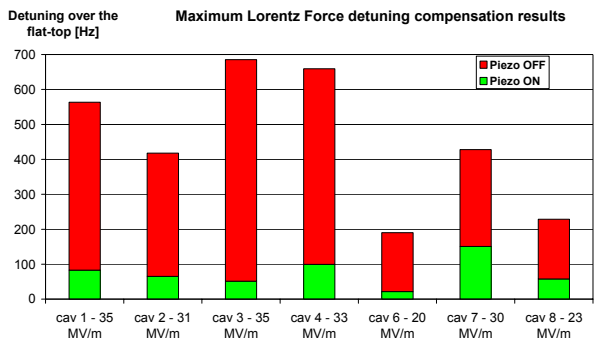

Figure 3: The results of detuning compensation.

The piezo sensor response for cavity 5 was too small to be analyzed. Moreover, a strange behavior of the piezostack was noticed. The best results of active Lorenz force compensation was observed for cavities 1, 3 and 4 which were detuned at gradients of 35 MV/m. The detuning over the flat top region for cavity 3 was decreased from around 700 Hz down to 50 Hz.

For the digital control system test purposes, a simple cavity simulator has been developed. The raw data sampled from the operational system are taken from DOOCS servers. The samples are stored in internal BRAM memory blocks of Virtex II Pro FPGA. The system is driven by a trigger signal with flexible range (2-10Hz) repetition rate, as in the RF pulse operating mode. A strobe signal with 1 μs period time is also added. The simulation data can be easily changed using a C++ control application running on embedded Sparc computer. The system also contains a MUX, which allows selecting the results from various processing blocks. The results can be easily analyzed using Matlab environment. The detuning signals for cavities 1, 2 and 3 are shown in Fig. 4.

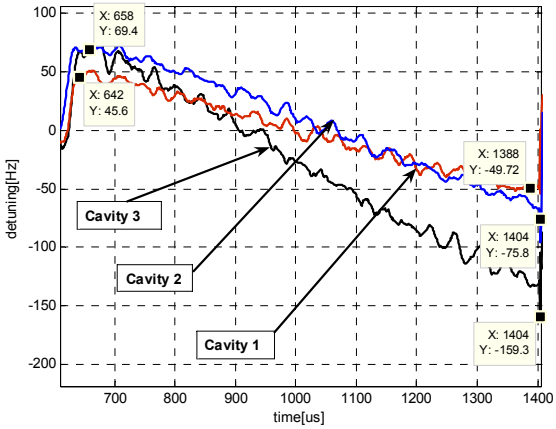

Figure 4: Cavity detuning computations using Simcon3.1L simulator – flat-top region.

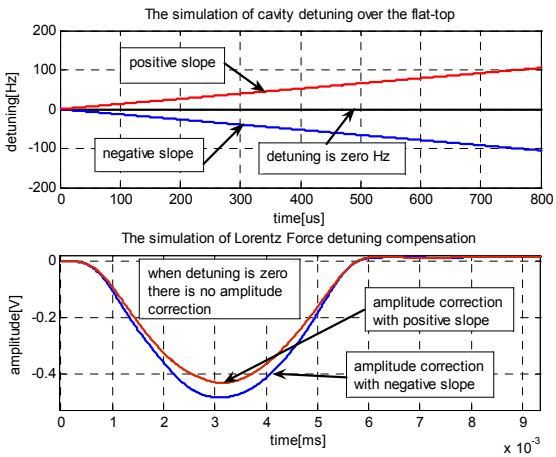

Figure 5: Amplitude correction simulation results using Simcon3.1L simulator.

Moreover the first hardware tests of adaptive feed-forward algorithm have been carried out (see Fig. 5). The detuning over the flat top has been modeled as a linear function with positive, negative and zero value of the slope. When the slope is positive the driving signal amplitude is decreased while the value is negative the amplitude is increased. The amplitude correction is finished when slope value is equal to zero value.

Implemented hardware simulator has been successfully tested with real probe signals from Module ACC7 in MTS. The proper detuning signal for cavity 7 has been measured online using fast DOOCS servers. Moreover the control system has been equipped with 32 KB internal memory block for recording cavity oscillations without piezostack's pulse (microphonics) with a long time period around 300 ms (see Fig. 6).

The main resonance has been noticed around 400 Hz, 700 Hz, 1 kHz, 1.3 kHz, 1.6 kHz, 1.9 kHz. The higher frequencies could be caused by other cavities and need more attention.

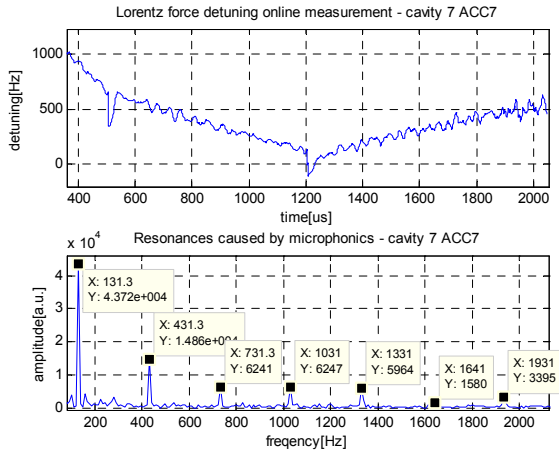

Figure 6: Online measurements of cavity detuning(upper) and fft analyze of cavity 7 ringings.

CONCLUSION

- An FPGA-based control system for active detuning compensation has been successfully demonstrated.
- The implemented VHDL components have been optimized for minimum latency and resource utilization. They were used to compute reference signal error (detuning) for adaptive feed-forward algorithm development.
- The measurements performed show that the Lorentz force detuning is decreased by factor 5.
- The implemented hardware simulator can be easily used to test and discover new algorithms i.e. for microphonics compensation.

ACKNOWLEDGEMENT

We acknowledge the support of the European Community-Research Infrastructure Activity under the FP6 "Structuring the European Research Area" program (CARE, contract number RII3-CT-2003-506395), and Polish National Science Council Grant"138/E-370/SPB/6.PR UE/DIE 354/2004-2007".

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