Production errors & improvement of our quality standards

Quality Management for XFEL Series Production

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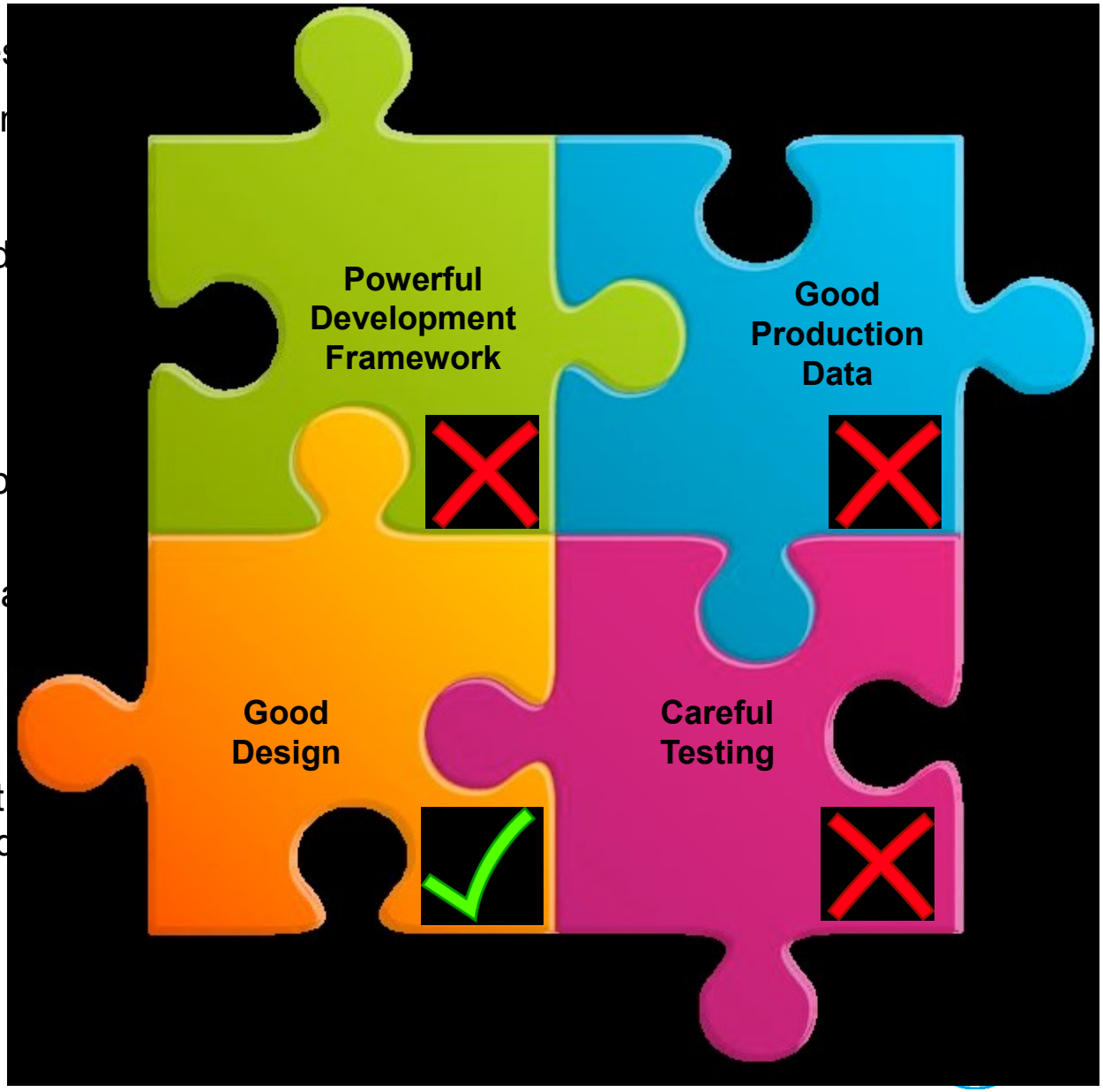
Warsaw, 10.06.2014

HELMHOLTZ ASSOCIATION

DESY

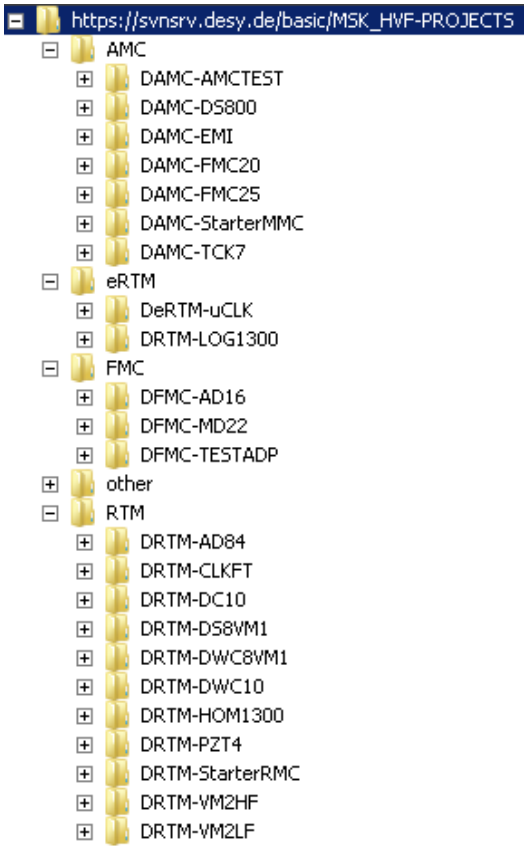
Introduction

- Development focus is on des
- Challenge: Series productio
- Observations:
  - Mistakes are discovered „Production revision“
  - Issues forgotten in new revision
  - Problem with reproducib and repeatability
  - Difficult to find data (“fin
  - No History
- Simple mistakes are difficult handle if we have 50+ Boar 50.000+ Euro costs



Development Framework: SVN

- Use SVN for design data storage
- Provides backup, sync., traceability, history, freezing
- “Living” files (Altium, mechanics, firmware) go to SVN
- “Dead” data (e.g. data sheets, measurement data) goes to N drive
- Do not put trash (e.g. temp) files there to SVN
- Commit regularly (e.g. every day), use a verb in commit text
- Each Project shall have branches, tags and trunk
  - Trunk is the design in progress
  - Tag: Create it whenever a board arrives (for each physical board we shall have a tag)
  - Branches: Are different versions and modifications (e.g. FRED3M)



- https://svnsrv.desy.de/basic/MSK_PROJECTS/
- https://svnsrv.desy.de/basic/MSK_HVF-PROJECTS/

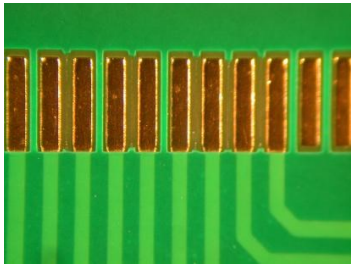
Development Framework

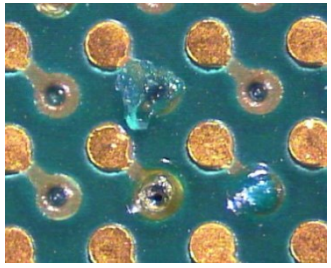
- Use Altium Vault as the only library for new (!) designs
  - Clean library can avoid manufacturing issues, reworks and redesigns
  - Provides traceability and history and update of faulty components
  - Provides clean BOM and Assembly plots with no extra effort
  - Managed by Robert (applies common rules)
  - Adoption of shared library is an iterative process.

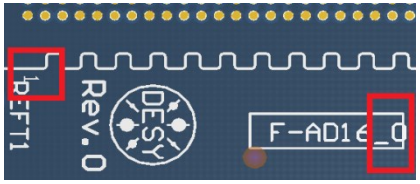
- Laboratories
  - Order replacement when you use something up!
  - We will install a list of missing things that have to be ordered
  - If you take something away, please leave a note
  - JTAG adapters are now personal – do not steal them

Design

- Schematics
  - Please use proper templates and deliver clean schematics.
  - Use comments in schematics. (Avoid red color for comments)
  - Do ERC and review the problems
  - Define all components, at least by „best guess“ – no „undefined“ parts
- PCB
  - Boards shall have no DRC mistakes (sometimes very few are acceptable)
  - Prepare fabrication information.
- Variants: Keep Number of Variants as low as possible. Document Differences



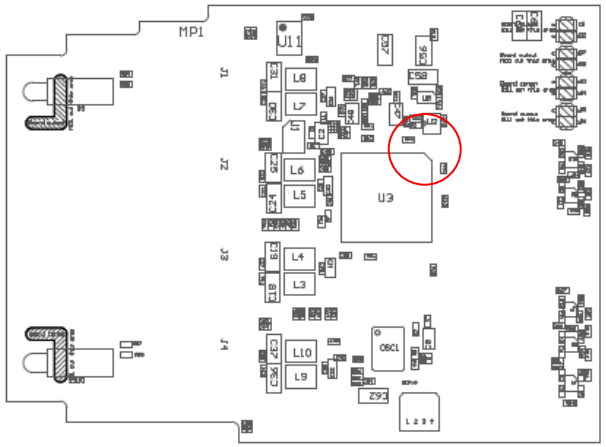




Production – Many issues because of non-precise data

- Please review all the production files.
  - Avoid unnecessary files. All has to be consistent & correct.
  - Include impedance, material, surface Information.
- **Review BOM. Provide exact manufacturer and part number**
  - Ordering numbers are optional. If you have them, make sure they are correct
  - Mark components that can be replaced with generic ones
- **Provide assembly drawing as PDF !!!**
  - Usually 4 pages (Designators and values top/bottom) - Check Pin 1 Marking!
  - Include Manufacturer instructions. (e.g. hand soldering)
- Board shall come from one hand
  - Ask assembly company to order parts and PCB.
- TAG received Boards

Assembly drawing



Docoument Template + Board Information

Board Outline + Board Cutout

Top Designators

Board Thickness: 1.6mm
Layer Count: 6
Layer Stackup: Accrording to attachment
Board Material: Standard FR4
Smalltest Track: 100um
Smallest Hole: 0.2mm
Surface: NiAu
Print Overlay (Silkscreen): no
Board Outline: Milled
Impedances: Only Layer 5, differential 100 Ohm
100R Configuration: Diff. GCPW 400-100/100/100-400, see attachment
Impedance Mesaurement report required: yes

CONFIDENTIAL MATERIAL

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TITLE:
DFMC-SFP4
Top Designators

DATE:
21.01.2015

LP NO.:
–

REV:
B

FILE NAME:
FMC_SFP4.PCBDOC

LP Type:
6 Layers

SCALE:
SCALE: 1.00

Board Testing

- Minimum: Check operation of all ICs (indirect check also ok)
- Report problems in Redmine
- Use stickers for marking boards (green/yellow/red/brown)

#	Tracker	Status	Priority	Subject
1495	Bug	New	Normal	Isolating Tape needed on green LED unter FP Mechanics
1494	Improvement	New	Normal	Rotate all Texts on PCB to be redeable when in crate
1493	Bug	New	Normal	DCDC Switching Frequency is too low
1492	Bug	New	Normal	Modification for IPMI access from CPLD
1491	Bug	New	Normal	Ground unused MCU pin for revision detection
1490	Improvement	New	Normal	DDR2 memory differential clock termination wrong
1396	Bug	New	Normal	Front Panel Holes for Light Pipes are too big
1393	Bug	New	Normal	FMC1 presence pullup is wrong

FMC25 Test Report

Region	Designa	Test	Value/Result	Remark
FPGA				
	IC5	JTAG Accessibility of Virtex-5	works at 12 MHz	verify with ISE at 12 MHz
	IC5	PCIe function	PCIe x4 works	verify with application
	IC5	P2P Links		test all links (put 2 boards in crate, verify with IBERT, note BER)
	IC5	MLVDS Links		Toggle Levels at max rate with FPGA, verify with scope
	U9	Reference Voltage	2.49V	verify with scope, note voltage level
	IC19	JTAG Accessibility of Spartan-6	works at 12 MHz	verify with ISE at 12 MHz
CPLD	IC6	JTAG accessibility	works at 12 MHz	verify with ISE at 12 MHz
	U30	SPI Flash	works	program FPGA image at max config rate and max bus width
	U19	SPI Flash	works	program FPGA image at max config rate and max bus width
USB	IC23	Communication with MMC, SP6	works at 115200	verify simple Communication with Terminal
	U35	Eeprom for USB	works	Generate File and Download , put binary to SVN

Summary

- Mass production is a challenge
- We have to improve our procedures and production files to manage this
- We need traceability
- Use our framework (SVN, Redmine, Vault) - the team will benefits.

Requirements for Technosystem

- Do not produce a board where an assembly drawing is missing
- Do not use silkscreen for component orientation
- Replace only components marked as generic/ multicomp
- Request confirmation when changing non-generic parts
- Stop if board delaminates
- Provide an error report for each batch
- Do a simple visual check on all the boards

One Correction

- 200mVpp ripple coming out of each Voltage input on FRED2A, FRED2B.
- Solved in FRED2C, FRED3x.