

PZ16M status and plans

2015 MSK collaboration workshop

Julien Branlard

PZ16M status and plans

ISE, Warsaw, 12.06.2015

Last slide from last year's PZ16M presentation



■ Ship unit sample ITech

- Include new PBE panels, new plates, new BOM, new documentation, new test firmware
- Assembly of 4 remaining units
- Extra cost due to DESY design change requests

DONE

DONE

PAID

■ Evaluation of modification list for current PCB

- Triggered for safety reasons (FPGA cold override CRYO OK)
- Stay with minor modifications (avoid several production cycles)
- BUT wish list is growing

DONE




































■ Next step:

- Review proposal
- Launch production and call for tender

ON GOING



WORK DONE IN THE LAST YEAR: meetings...

 2014_01_20 - PZ16M meeting minutes.docx	1/21/2014 2:44 PM	Microsoft Word-D...	106 KB
 2014_04_17 - PCB Modifications for PZ16M.docx	4/17/2014 5:11 PM	Microsoft Word-D...	288 KB
 2014_04_17 - PZ16M meeting minutes.docx	4/17/2014 2:45 PM	Microsoft Word-D...	125 KB
 2014_04_24 - PZ16M meeting - independent hardware monitoring.docx	4/25/2014 11:15 AM	Microsoft Word-D...	18 KB
 2014_04_25 - PCB Modifications for PZ16M.docx	4/25/2014 11:11 AM	Microsoft Word-D...	371 KB
 2014_04_30 - PZ16M meeting minutes.docx	5/7/2014 11:29 AM	Microsoft Word-D...	23 KB
 2014_05_08 - PZ16M meeting minutes.docx	5/8/2014 11:50 PM	Microsoft Word-D...	74 KB
 2014_05_15 - PZ16M meeting preparation for ITech shipment.docx	5/15/2014 4:22 PM	Microsoft Word-D...	18 KB
 2014_06_12 - PZ16M meeting.docx	6/12/2014 5:34 PM	Microsoft Word-D...	20 KB
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 2014_07_03 - PZ16M meeting.docx	7/3/2014 12:45 PM	Microsoft Word-D...	30 KB
 2014_07_08 - PZ16M meetings.docx	10/2/2014 3:28 PM	Microsoft Word-D...	276 KB
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 2014_09_25 - PZ16M meeting minutes.docx	9/25/2014 12:55 PM	Microsoft Word-D...	21 KB
 2014_10_02 - PZ16M meeting minutes.docx	10/2/2014 6:21 PM	Microsoft Word-D...	24 KB
 2014_10_08 - Modifications list for the new PZ16M PCB.docx	10/8/2014 11:22 PM	Microsoft Word-D...	398 KB
 2014_10_16 - PZ16M review with ITech.docx	10/20/2014 10:47 ...	Microsoft Word-D...	21 KB
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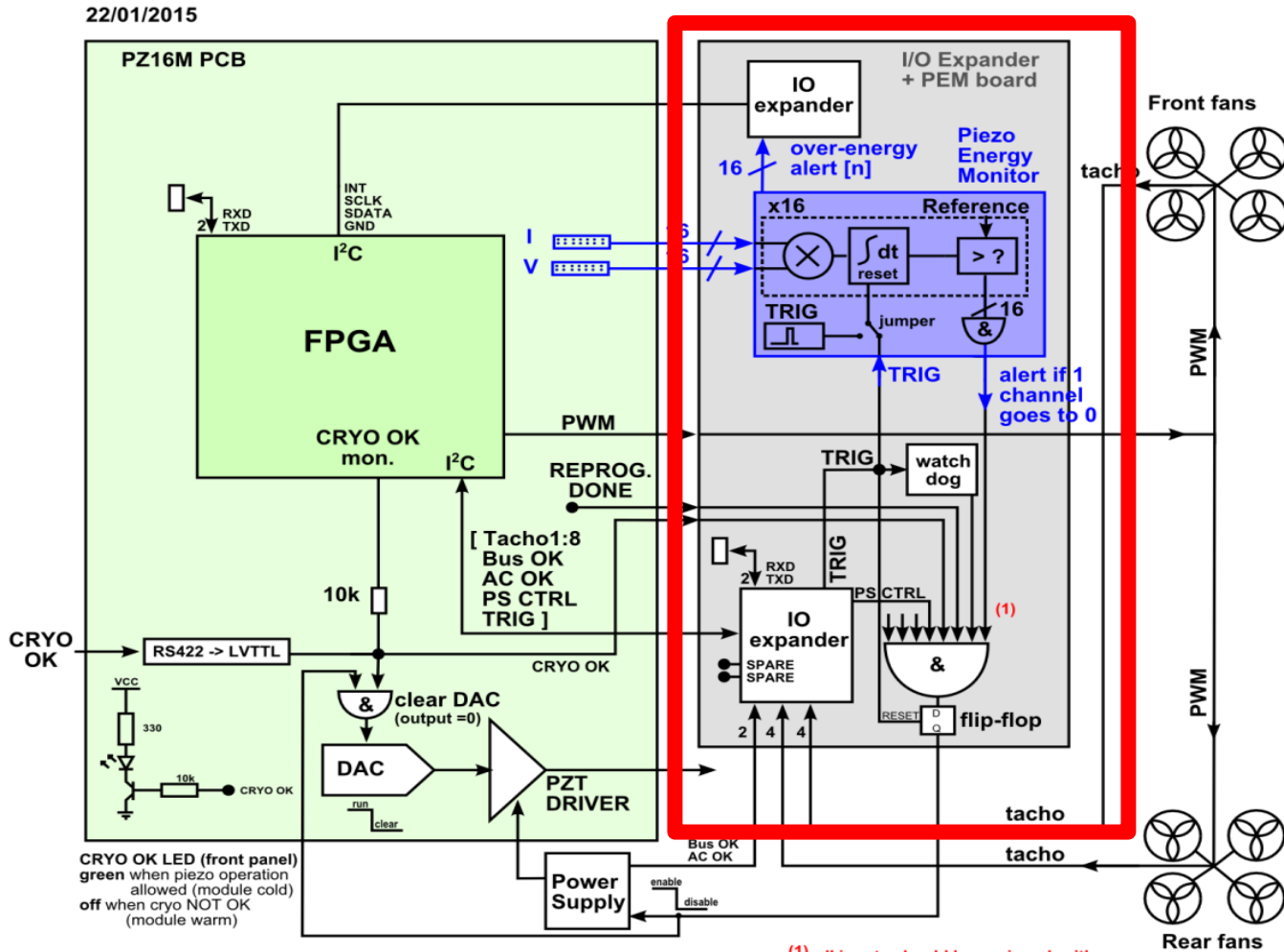
> The PZ16M team

- **Marcin Chojnacki**
- **Mariusz Grecki**
- **Konrad Przygoda**
- **Henning Weddig**
- **Julien Branlard**
- **with reviewing help from Michael Fenner**



WORK DONE IN THE LAST YEAR: PEM

> Piezo Energy Monitoring (PEM) board



WORK DONE IN THE LAST YEAR: PEM

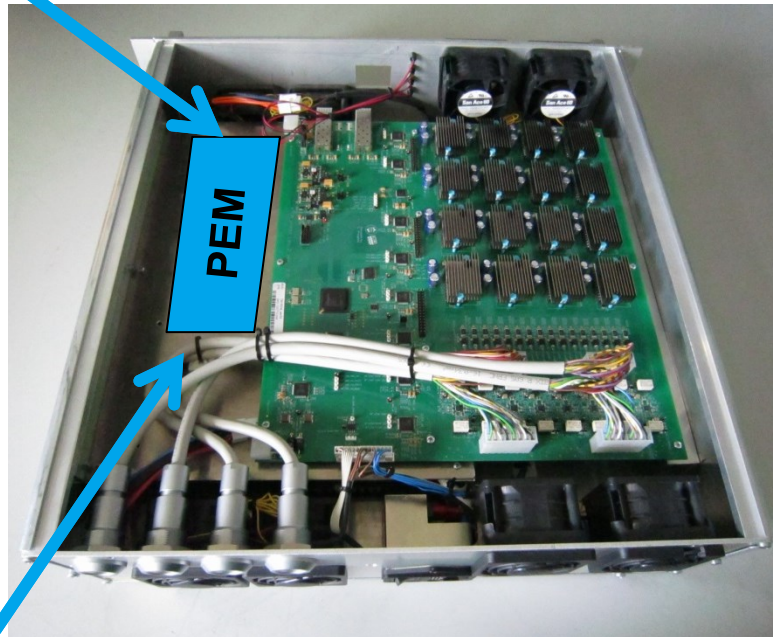
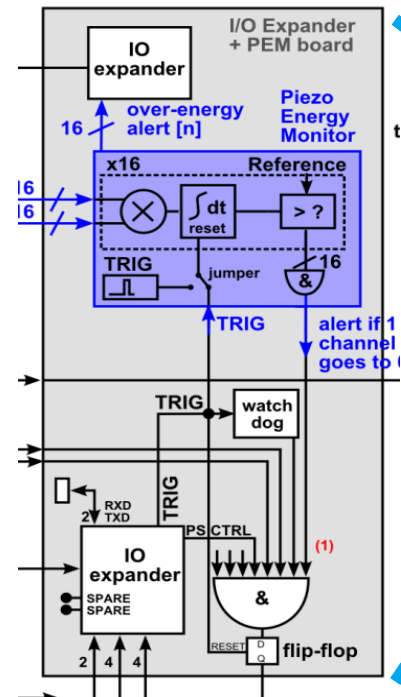
- Schematic reviewed done
- PCB layout (2-3 weeks)
- PCB review in July
- Production and tests after September

PEM schematic review

1. General comment:
 - a. Add top level block diagram on one sheet
 - b. Recommendation: if possible add section of block diagram on corresponding sheet
2. Added connectors to connect to main PCB
 - a. Please include manufacturer's name (copy-paste how it was done for other board)
3. Multipliers/integrator/comparator
 - a. Resistor instead of potentiometer is good
4. Tap points
 - a. Two different type of tap points were used, according to Henning's schematic
 - b. (smd or through hole) → good
5. Over current circuit protection
 - a. OK
6. All this circuit has to be multiplied 16 times
 - a. EXCEPT reset circuitry
 - b. Use one sheet per channel
 - c. Use separate sheet for reset circuitry
7. "Top" IO expander
 - a. Should be address 1
 - b. Remove resistors to ground for A1/A2
 - c. Place 10k pull up for A0
 - d. Add 33 Ohm serial resistor for each leg going to the And gate at output of PEM in case traces are long (clarify with Michael Fenner if this is needed)
8. Trigger section going to monoflop
 - a. Only 1x (remove from 16 channel)
 - b. Verify connection with TRIG select
 - c. Open question about diode in // with R going to VCC (is this correct?)
9. "low" IO expander
 - a. A0/A1/A2 → should be address 0
 - b. Place PWM and IO on separate sheet
 - c. Pull-up R on tachometer signal OK (check spec sheet to see if use 330R or 1k)
 - d. Ohm resistor on tachometer lines
 - i. only for prototype, remove now
 - ii. Remove labels
10. AND at output of PEM
 - a. Keep pull-up and pull down in case AND logic is changed
11. Watchdog
 - a. Check circuitry with Mariusz Grecki

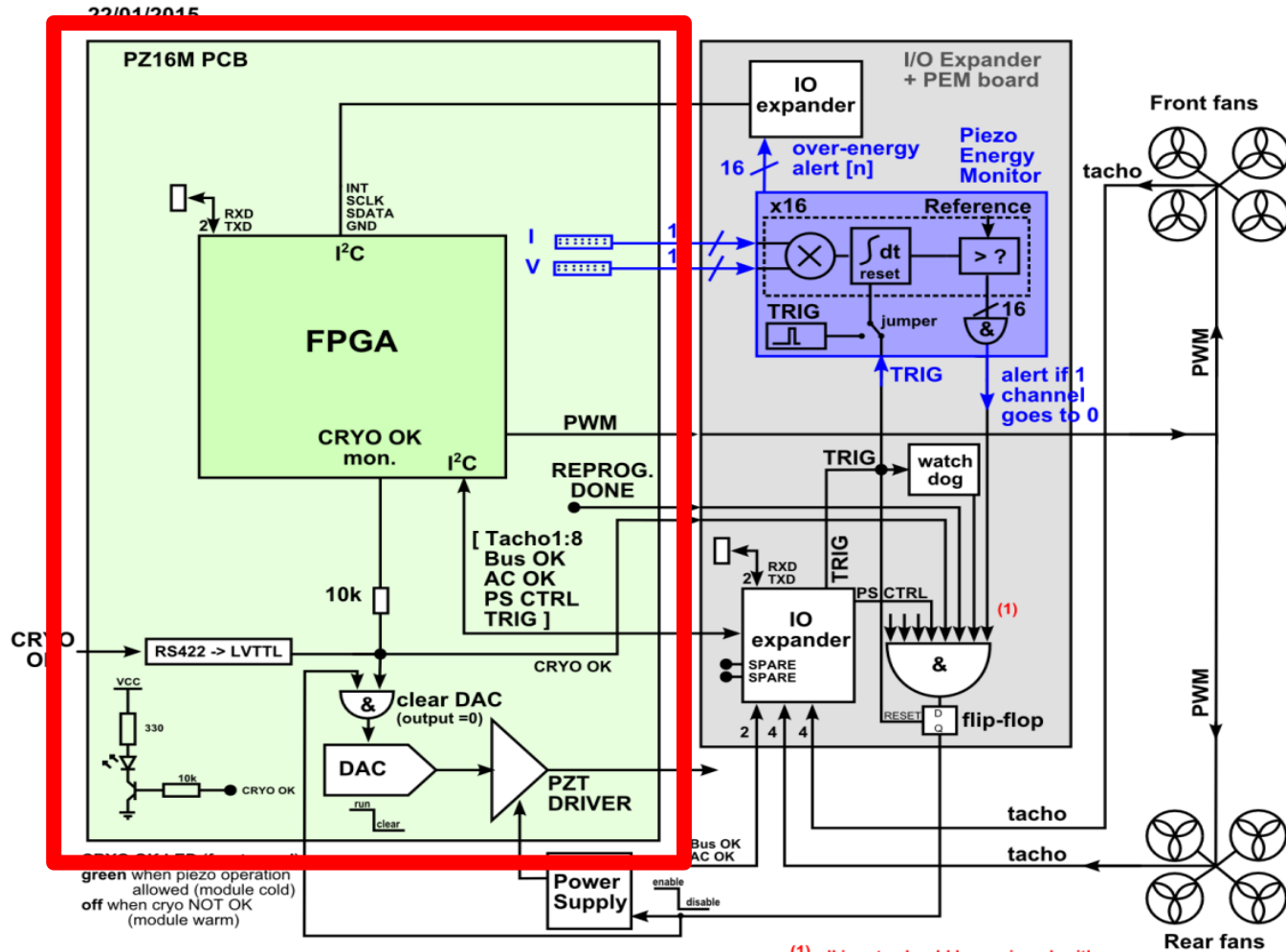
Final remarks

- Marcin can implement all changes for next week
- Upload to SVN
- When approved, PEM PCB layout work can continue
- No meeting next week due to the MSK collaboration workshop
- Marcin might come to DESY in July


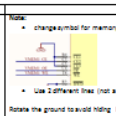
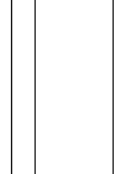

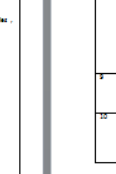

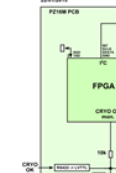
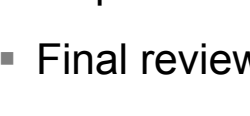


WORK DONE IN THE LAST YEAR: main PCB

> PZ16M main PCB



WORK DONE IN THE LAST YEAR: main PCB

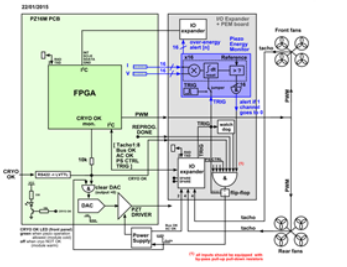
Point	Description	Status
5	MAIN PCB modifications	
1	Check the SW2 pin connector to be able to locate CR10 OK connector on the main PCB.	Done Note: • Signal not needed for loading DAC. • Missing connection from CR10 OK to PDM1/2/3/4 board. • Clear-DAC (required clear) Connect the DAC. • CR10 OK connector after too loose: adjust control going to AIO. • Replace the SW22 connector to a reliable version (SW1 + schematic component change id: SW25VU222 new: SW25VU23) • The output of the SW222 relative either is high when code is disconnected → clean linear attractive but better (DONE) or low when high when code is disconnected (DONE) CR10 OK connector needs to be replaced (due to the presence of flux) → (Check & include in documentation) • As a consequence if you're not OK, or code disconnected or shorted, the wire either will support 5V, inverted to 0-9 clear-DAC and display 9S (good) Solution to bypass cr10 OK by using jumper could be done either inside the box or on the PCB connector outside by using a modified LEDS plug (one of the pin must be grounded)  5V will check which pin needs to be grounded.
2	Place a new LED for CR10 OK illuminated in the back diagram.	Done Note: • change name LED_OK and LED_OK_FULL to LED_OK and LED_OK_FULL → DONE • LED_OK notes break connection when changing names → no more needed
3	CONNECT CR10 OK lines on ADC (this should)	Done
6	Control of digital SRAM memory (required an additional pin)	Done Note: • change symbol for memory chip selects  • Use 2 different lines (not an inverter) • Use same pins, each going to a separate chip Rotate the ground to avoid hiding label DONE
7	ADD a 2-layer capacitor to the main FPGA for decoupling purpose.	Done Note: • Remove old comments (pin missing) → DONE • Pin missing always top side of firmware will need to be added • Change red comments to black (red means wrong) → DONE 1. Requires 3 free pins from the FPGA → OK from SW10 2 2. Use a 2-pin connector (SW10: SW10) 3 3. Use good pin connector single row
8	ADD a 2-layer capacitor to the SW10 supply capacitor for transient and resistor for DCClear.	Done Note: • These 2-layer capacitors should be changed to 10V unidirectional  • DONE a. Top and bottom 2-layer should be replaced with 2 diodes in anti-parallel, 12V each
9	ADD a 2-layer capacitor to the SW10 supply capacitor for transient and resistor for DCClear.	Done Note: • These 2-layer capacitors should be changed to 10V unidirectional  • DONE b. Top and bottom 2-layer should be replaced with 2 diodes in anti-parallel, 12V each
10	ADD a 2-layer capacitor to the SW10 supply capacitor for transient and resistor for DCClear.	Done Note: • These 2-layer capacitors should be changed to 10V unidirectional  • DONE b. Top and bottom 2-layer should be replaced with 2 diodes in anti-parallel, 12V each
11	Routing trace should be widened (80%)	Done
12	Routing components close to mounting hole should be moved further away.	Done Note: • Easier from layout point of view to stay with 4 connectors the routing the connectors by 90 degrees is not trivial → stay with current configuration Propose: stay with current orientation but move all 4 connectors to the right (1cm towards ADC) should help with air flow → DONE  Alternative - move PC board original position - make
13	Change connector type (use led 125PFA and 125L125 for FPGA boot)	After talking with TM, decision has not to do it
14	Add a 2-layer capacitor to the SW10 supply capacitor for transient and resistor for DCClear.	Propose Alternative - move PC board original position - make
15	Change connector type (use led 125PFA and 125L125 for FPGA boot)	Done Note: • Change for pin (SW10) from and near CR10
16	3-pin will be spread out from 2 pins on PDM1 board. CR10 should be a "leaf" connector instead of direct - heat dissipation during soldering.	Done Note: • Voltage on PDM1 (V and 2-3V) • Connectors between main PCB and PDM1 • Use digital signal separated from supplies • Use 3-pin for each board supply → 3-pin connector (done on schematic) Better to locate voltage from signal Use 3-pin connector here as well → DONE
17	Move connectors from edge (2 and 3 pin) CR10 remain on the edge but not too close	Done Note: • Rotate 180 degree to be consistent with orientation of other connectors • CR10 connector use one use (single) here as well → DONE
18	SPF10 connector on main PCB	Done Note: • This is a problem with the new chassis size (SW10) in the main PDM1 board. There is enough space to track/remove optical flow. Check dimension and description in documentation
19	Relating CR10 OK connector to help air flow	Done Note: • This is a problem with the new chassis size (SW10) in the main PDM1 board. There is enough space to track/remove optical flow. Check dimension and description in documentation
20	ADD AN102 to clear DAC output (available the DAC to prevent latching of the driver when no high will keep a presence)	Done
21	ADD jumper to bypass clear DAC	Done Note: • SW10 output of SW20 2 pin • Jumper to bypass the SW10 output when code is disconnected: wire a jumper through a resistor (to force 1) → Check and done
22	Group connections to expand 1 0-5V to force CR10 OK (2-layer, PROD_DONE)	Done
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22	Group connections to expand 1 0-5V to force CR10 OK (2-layer, PROD_DONE)	Done

SW10 connector
→ DONE (check 10-pin)

Note: use 125PFA control on main PCB as backup

Replace 2-layer capacitor

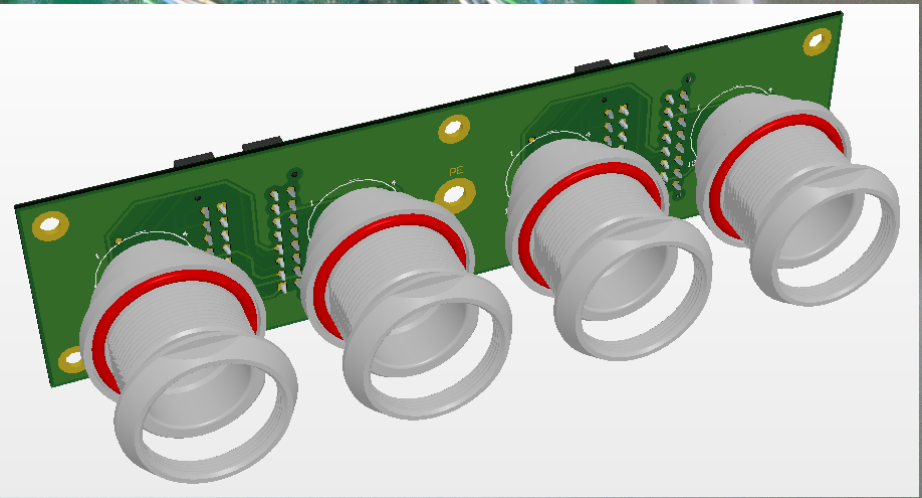
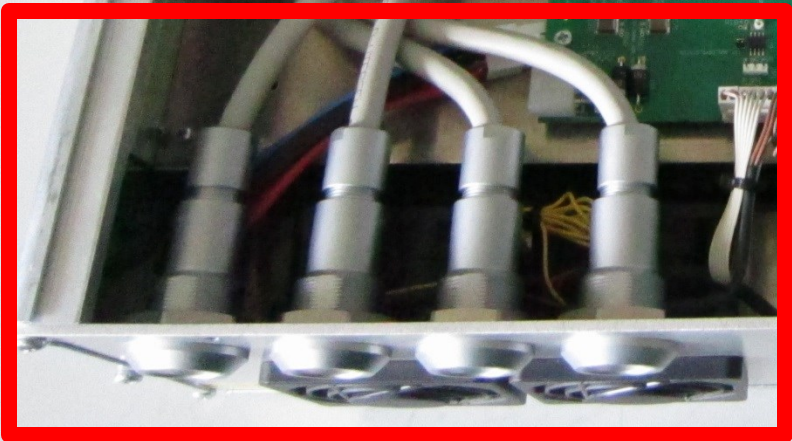
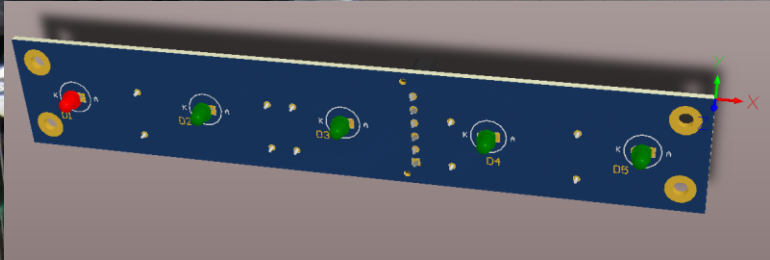
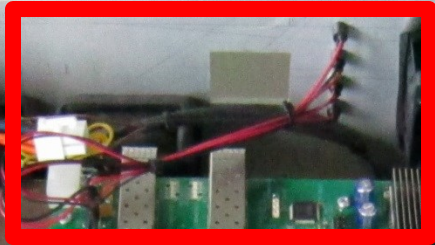
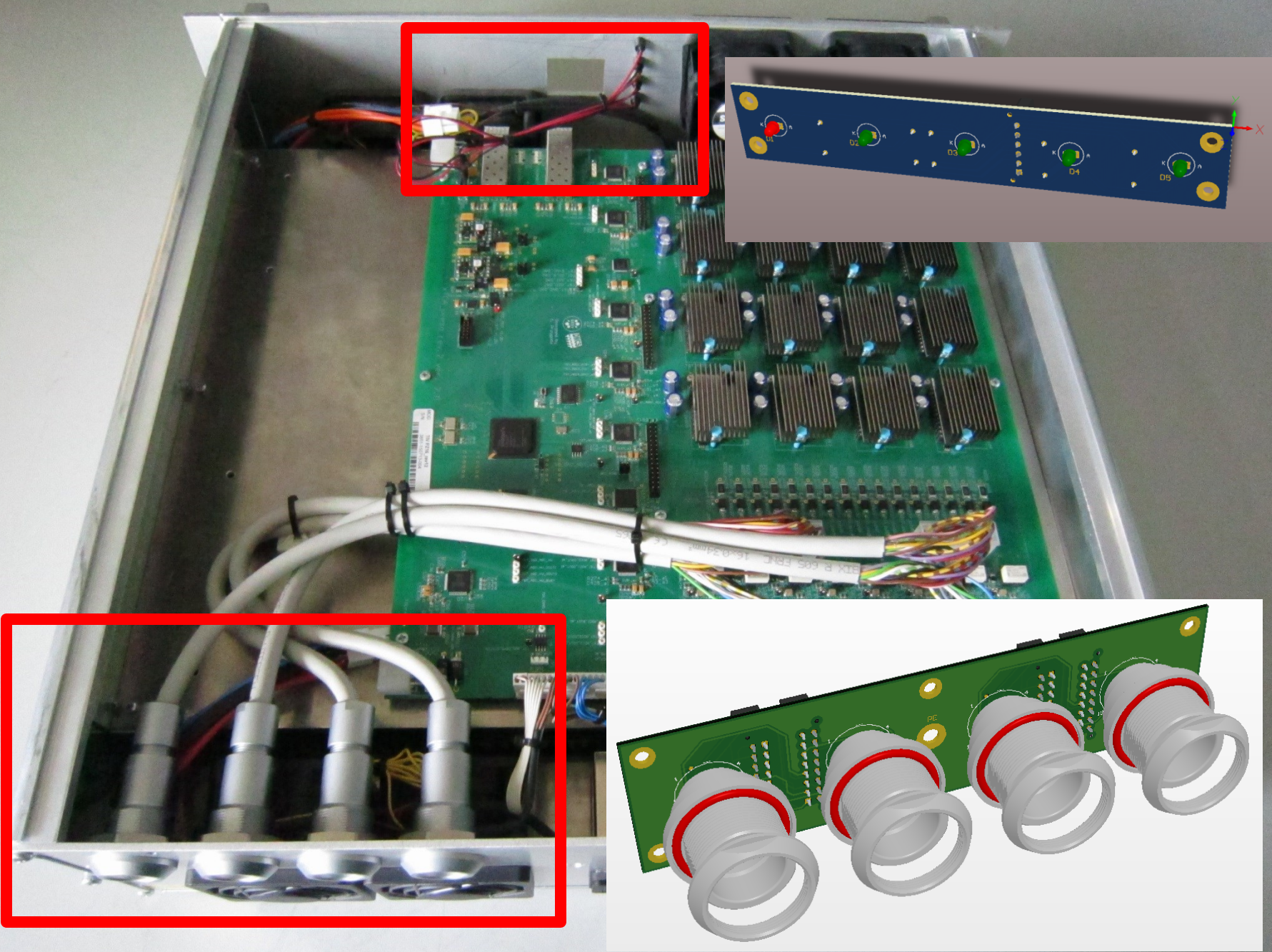
- In parallel with other capacitors, higher R value will provide a lower self-resonance, allowing to operate at higher frequency microchips
- Can be placed in DUTS
- NG check parameters



> Main PCB update

- 22 points corrected and reviewed
- Final review pending
- Production of 1-2 prototypes
- Tests
- Revision ?
- Launch call for tender

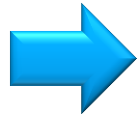




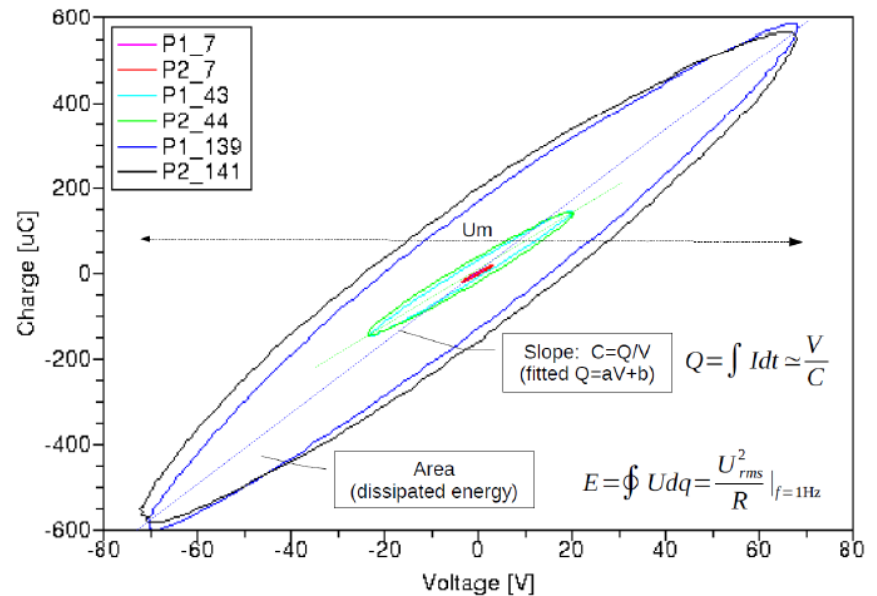
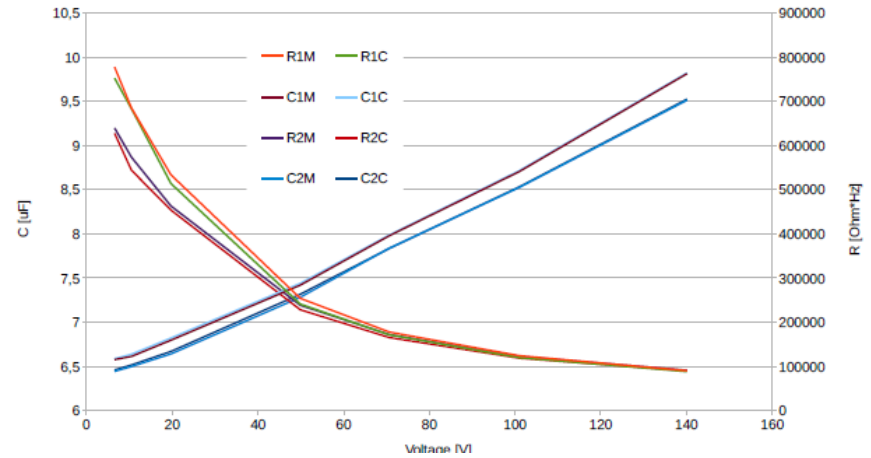
WORK DONE IN THE LAST YEAR: firmware

High Level Design of Piezo Energy, Temperature and Impedance Computation

Date: 13/3/2015
 Revision: 1.2
 Author: Mariusz Grecki



Mariusz Grecki,
 Bin Yang,
 Lukasz Butkowski,
 Julien Branlard



NEXT STEPS (what we did wrong / where we need to improve)

> Careful review of BOM

> Careful review of production data

> Mechanical integration

- Created problems during the last production batch with ITech
- **No 3D model, no accurate 2D plans**
- Do we try production without ? → man power issue

> Schedule

- Sep. 15: Production of next version PZ16M prototype (PZ16M version2)
- Dec. 15: Deadline for validation of PZ16M-v2
- Jan.-Jun.16: Purchasing, production of PZ16M
- July 16: Installation/commissioning of PZ16M (too late!)

Optimistic:
Pessimistic:

small margin to get it done in time
we are already too late, we might have to install PZ16M after cool down

THANK YOU!

