ESTIMATION OF IQ VECTOR COMPONENTS OF RF FIELD - THEORY AND IMPLEMENTATION

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ABSTRACT: This paper presents the mathematical algorithm of RF-field IQ vector estimation and its VHDL implementation. The model is implemented in MATLAB and used to optimize system parameters (intermediate frequency and sampling rate). Model takes into account the finite accuracy of ADCs, the non-linearity of ADCs characteristics and also voltage and jitter noises. The VHDL implementation of the algorithm and its functional verification is presented.

INTRODUCTION

High-energy accelerators use Radio Frequency (RF) field to accelerate charged particles. Measurements of effective field parameters (amplitude and phase) are tasks of great importance in these facilities. The digital control system has to assure regulation accuracy better than 0.01% in amplitude and 0.01 degree in phase (EU-XFEL requirements) [1]. The block diagram of the control system for the accelerator LLRF (Low Level Radio Frequency) subsystem is presented in Fig.1 [1]. This is a typical closed-loop feedback regulation system attempting to keep the amplitude and phase of the RF signal in the accelerating cavities on a given level. The RF signal is downconverted in frequency but keeping the information about amplitude and phase and afterwards sampled in ADCs. One of the several tasks for FPGA is to estimate the amplitude and phase of the RF signal. Those parameters are further used in control algorithm. Therefore it is important to obtain their accurate values [2]. The optimal ADC sampling rate and intermediate frequency should be chosen in order to minimize disturbances from noise, clock jitter and nonlinearities of components' characteristics.

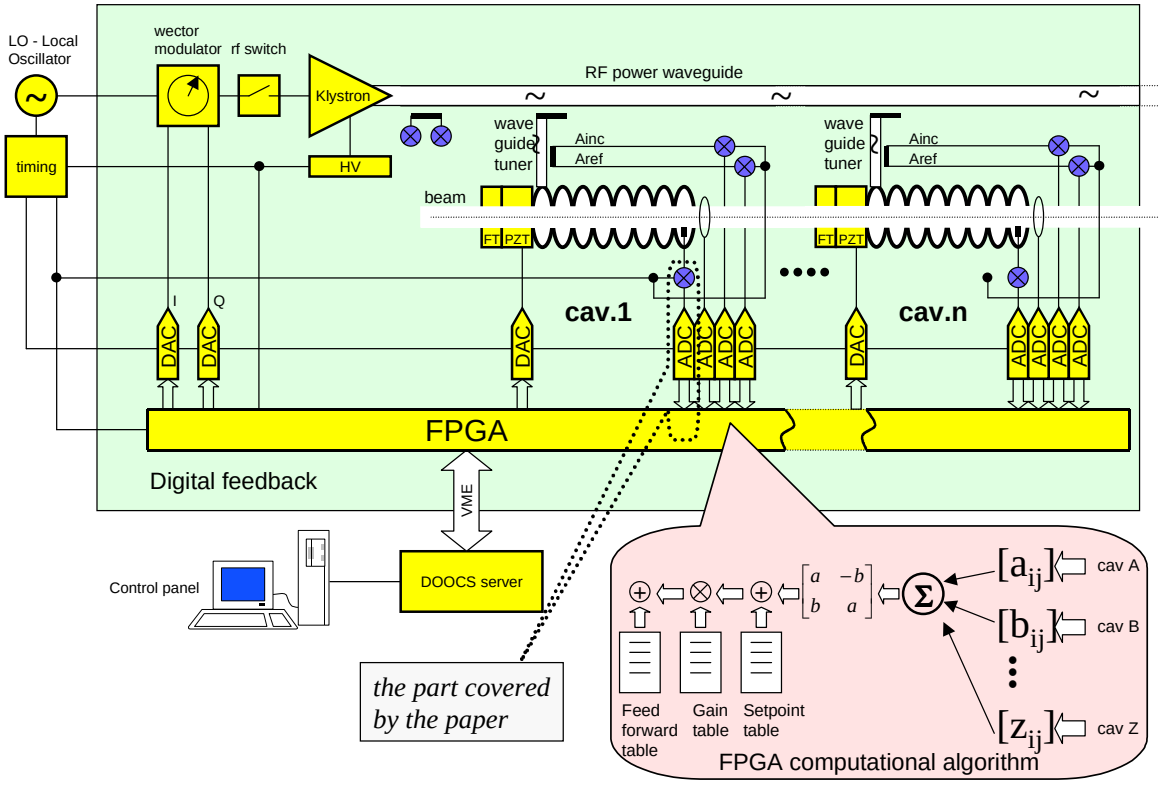

Fig. 1. Block diagram of the LLRF control system

MATHEMATICAL ALGORITHM

The downconversion process can be performed by nonlinear mixers multiplying RF signal and reference signal (Fig. 2). This operation shifts frequency spectrum of the signal preserving unchanged information about amplitude and phase of RF field.

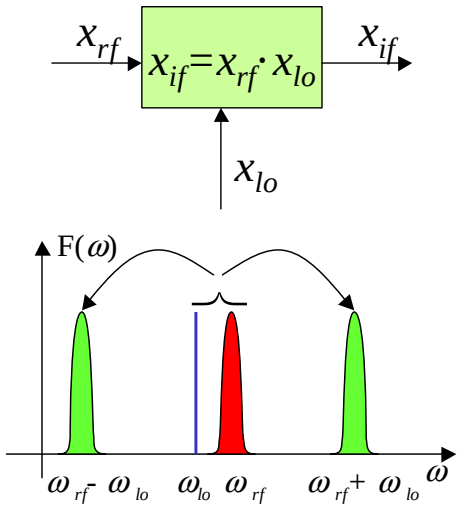

Fig. 2. Mixer and downconversion of signal spectrum

An ideal mixer produces nothing but the mathematical product of two input signals at its output. Let (according to eq. 1) x_{rf} and x_{lo} be respectively the RF and the Local Oscillator signals at the two inputs of the mixer.

$$\begin{aligned} x_{rf}(t) &= A_{rf}(t)\sin(\omega_{rf}t+\psi(t)) \\ x_{lo}(t) &= A_{lo}\sin(\omega_{lo}t+\psi_{lo}) \\ \omega_{if} &= \omega_{rf}-\omega_{lo} \end{aligned} \tag{1}$$

Following trigonometric laws the product of these two signals is given by eq.2:

$$\begin{aligned} x_{if}(t) = \frac{1}{2}A_{rf}(t)A_{lo}[&\sin\left(\omega_{if}t+\psi(t)-\psi_{lo}+\frac{\pi}{2}\right)- \\ &\cos\left((\omega_{rf}+\omega_{lo})t+\psi(t)+\psi_{lo}\right)] \end{aligned} \tag{2}$$

The higher frequency term is usually suppressed by appropriate analogue filtering, leading to signal with intermediate frequency (*IF*) given by eq. 3:

$$x_{if}(t) = \frac{1}{2}A_{rf}(t)A_{lo}\sin(\omega_{if}t+\psi(t)-\psi_{lo}+\pi/2) \tag{3}$$

Obviously, this signal contains the same amplitude $A_{rf}(t)$ and phase $\psi_{rf}(t)$ information as the RF-signal, except for an amplitude scaling by constant and arbitrary but constant phase difference. The signal with given amplitude and phase can be also seen as signal with two components: *I* and *Q* (**I**n phase and in **Q**uadrature - eq.4). For numerical calculations the IQ representation is more appropriate.

$$\begin{aligned} &x(t) = A\sin(\omega t+\varphi) = I\sin\omega t + Q\cos\omega t \\ &\text{where}: \quad A=\frac{1}{2}A_{rf}(t)A_{lo}, \quad \varphi=\psi_{rf}(t)-\psi_{lo}+\pi/2 \end{aligned} \tag{4}$$

The analogue signal *x(t)* is sampled by ADC with constant sampling rate. The task is to calculate from those samples the *I* and *Q* components. Let us assume that sampling rate is *SF* and intermediate frequency *IF*. It has to be assured that *M·IF=N·SF* (*M,N* –integer numbers) in order to perfectly synchronize the sampling process with *IF* signal. Therefore we obtain *N* samples of *IF* signal taken from *M* successive periods of the signal. The phase advance between two consecutive samples is $\Delta\varphi$ given by (5):

$$\Delta\varphi = 2\pi\frac{N}{M} = 2\pi\frac{IF}{SF} \tag{5}$$

For example, the intermediate frequency can be 81 MHz and the ADC is clocked at 36 MHz. The *N* and *M* are in this case 9 and 4 respectively. The phase advance between two consecutive samples will be in this case exactly 90°.

Taking N samples the equation set (5) can be written. Some Δφ (π, 2π..) lead to the singular equation set (5) and therefore those combination of *IF* and *SF* are not allowed.

$$\begin{aligned} x_1 &= I\sin\alpha_1 + Q\cos\alpha_1 \\ x_2 &= I\sin\alpha_2 + Q\cos\alpha_2 \\ &\ldots\ldots \\ x_M &= I\sin\alpha_M + Q\cos\alpha_M \end{aligned} \tag{5}$$

where $\alpha_i = \Delta\varphi\cdot i = 2\pi\frac{IF}{SF}i$

The set of N equations (5) has only two unknowns (I and Q) but the x_i samples differ from the real values because of sampling incorrectness. Taking into account more samples than is needed leads to statistical improvements of calculated I and Q values.

Application of the Least Square Method to the equation set (5) leads directly to surprisingly simple formula for I and Q (6). Details are enclosed in appendix.

$$\begin{aligned} I &= \frac{2}{N}\sum_{i=0}^{N-1}x_i\sin(i\alpha) \\ Q &= \frac{2}{N}\sum_{i=0}^{N-1}x_i\cos(i\alpha) \end{aligned} \tag{6}$$

As can be noticed from equations (6) the calculations need to use the sine and cosine tables of integer multiplicity of phase advance (eq. 5). Division in eq. 6 is only by the constant that can be simply realized in hardware. The sum in (6) reduces random sampling errors and also cancels constant offset.

VHDL IMPLEMENTATION

The algorithm presented in the paper was implemented as a design entity (Fig. 3) in Xilinx FPGA chip using VHDL description. The application of 14 bits ADC was

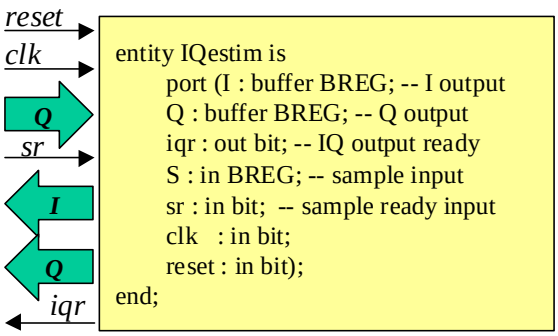

Fig. 3. The entity for IQ estimation (BREG is an integer type with the number of bits capable to fit samples from ADC)

assumed with 14 bits wide output signals I and Q however all internal calculation are done using integer arithmetic with 32 bits precision. The implemented design focus on speed utilizes two 18x18 bit multipliers, two 32bit wide accumulators, memory tables for sine and cosine values and some additional registers and flip-flops. That set of resources can be reduced if sequential operations are allowed – in this case IQ estimator needs only one multiplier and one 32 bits accumulator (together with additional logic and registers).

The designed VHDL entity (*IQestim*) was tested using Modelsim 5.8d simulator. For the test purpose a *test_iqestim* entity was worked out and applied. It uses text file as data source, read values of sampled signal from the data file, provide samples to the *Iqestim* module together with control signals and read calculated I and Q data. The tests of the *Iqestim* VHDL module proved the full agreement with expected results (Fig.4).

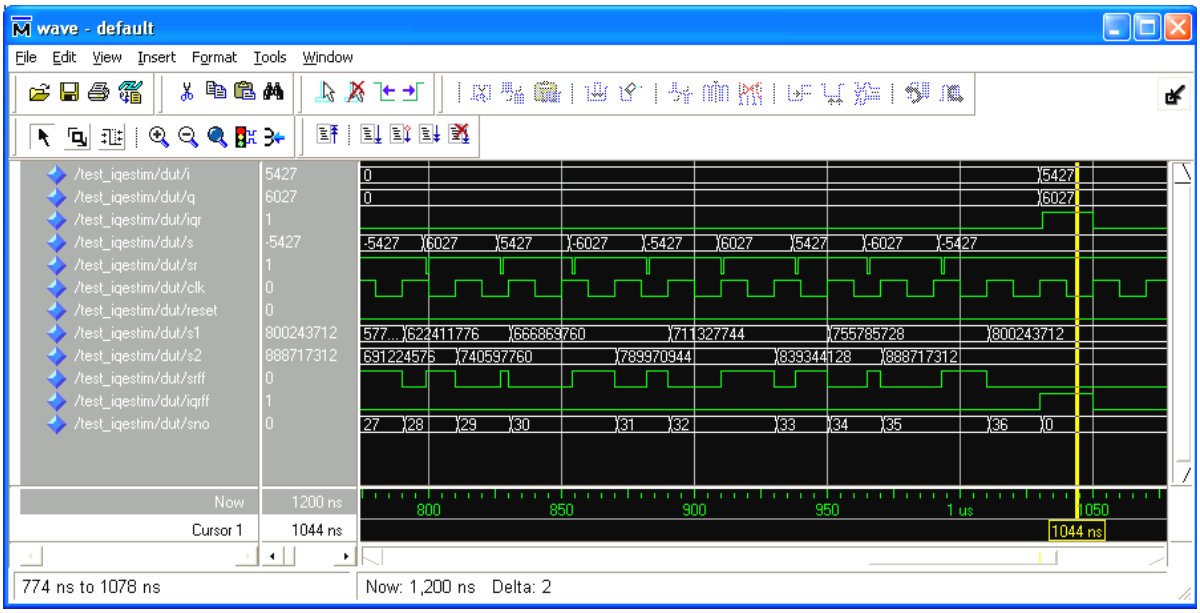

Fig. 4. IQ estimator (IQestim VHDL module) - simulation results
IF=81MHz, SF=36MHz time for sample collection -1μs therefore 36 samples taken into account
output: I=5427, Q=6027, => A=8110, φ=48°

PARAMETERS OPTIMIZATION

In real life signals are noisy and have offsets, clocks have a jitter, ADC and other components are not linear and introduce quantization errors [3,4]. All the facts should be taken into account, when designing the whole system. The important question to answer is how all the unavoidable troubles influence the accuracy of IQ estimator. In order to simulate the real conditions the Matlab application was written and several simulations for various parameters values were performed. All simulations were done for EU-XFEL [5] environment taking into account existing situation and planned changes. The computations were done using integer arithmetic, exactly the same way as in VHDL code. Noise and clock jitters with Gaussian distribution were taken into account in simulations as well as offset and differential and integral nonlinearity of the ADC. The output data from simulation are I and Q estimation errors. Also the statistical parameters (mean, standard deviation, min and max values) of errors are computed.

This Matlab application can be also used as a parameterized VHDL code generator. By clicking single button the VHDL description of the IQ estimator (*IQestim.vhd*) is saved in a disk file (the VHDL code is generated for chosen *IF*, *SF* and processing time). Generated code can be directly simulated and implemented in FPGA.

The Matlab model of the IQ estimator was used for evaluation of the idea and its properties. The computation was performed in the following way: for the intermediate frequency signal with the given amplitude and phase the signal samples were calculated taking into account nonlinear characteristic of the ADC, noise, jitter and offset. The "real" samples were processed in the estimation module and calculated I and Q values were used to obtain amplitude and phase. The two parameters were compared against given ones.

Sampling rate choice

For EU-XFEL accelerator the LLRF control system requires to calculate I and Q values every microsecond. Afterwards one cycle of sampling and IQ estimation should be repeated with 1MHz frequency. That means that ADC sampling rate should be integer multiplicity of 1MHz. However we need at least 3 samples to calculate IQ components (assuming constant repetition rate) so the minimum sampling rate is 3MHz. On the other hand the upper bound of ADC sampling rate is limited by the dynamic performance of ADCs and their accuracy (dependent on sampling rate). For nowadays ADCs one can assume the upper limit of sampling rate to be of order of 100MS/s. It is expected that faster sampling (resulting in higher numbers of samples) will allow to statistically improve the results of I and Q estimation as uncorrelated noise and jitters will compensate in the sum (eq.6). On the other hand faster sampling means less accurate sampling so the compromise needs to be searched for. For given intermediate frequency some of the sampling rates are not allowed since they lead to the phase advance 0° or 180°.

Intermediate frequency choice

There are also some limits in the case of intermediate frequency choice – it should also be an integer multiplicity of 1MHz. In the case of upper bound there is no strict limitation but jitters in clock signals reduce sampling accuracy for high intermediate frequencies. One should also take into account the limitations in Local Oscillator (LO) – some intermediate frequencies can be easier generated, some of them are more difficult to obtain. For the EU-XFEL control system IF=9MHz and 81MHz are directly accessible, but others can be also synthesized if there is a need.

Results of simulation

The ADC model used in simulation was based on AD6645 ADC from Analog Devices. The accuracy, nonlinearity and noise parameters were estimated on the base of its data sheet [6]. Also was assumed white noise from downconverter (0.5mV RMS) and clock jitters from local oscillator (stochastic gaussian distribution with standard deviation of 5ps). In every case the values of I and Q obtained from simulation were used to calculate amplitude and phase and result was compared to expected values.

The accuracy of IQ estimation in the presence of noise and clock jitters. At this stage of numerical experiments the ADC was assumed to be ideal (linear, without noise). Several simulations were performed to understand the influence of noises on IQ estimation accuracy for various intermediate frequency (9MHz and 81MHz) and sampling rate (various from 4MHz up to 100MHz). The results show that one obtains better accuracy with the given noise and clock jitters choosing higher sampling rate and lower intermediate frequency. The low intermediate frequency is particularly important in the presence of clock jitters. The characteristic of IQ estimation error for chosen parameters is presented in Fig. 5.

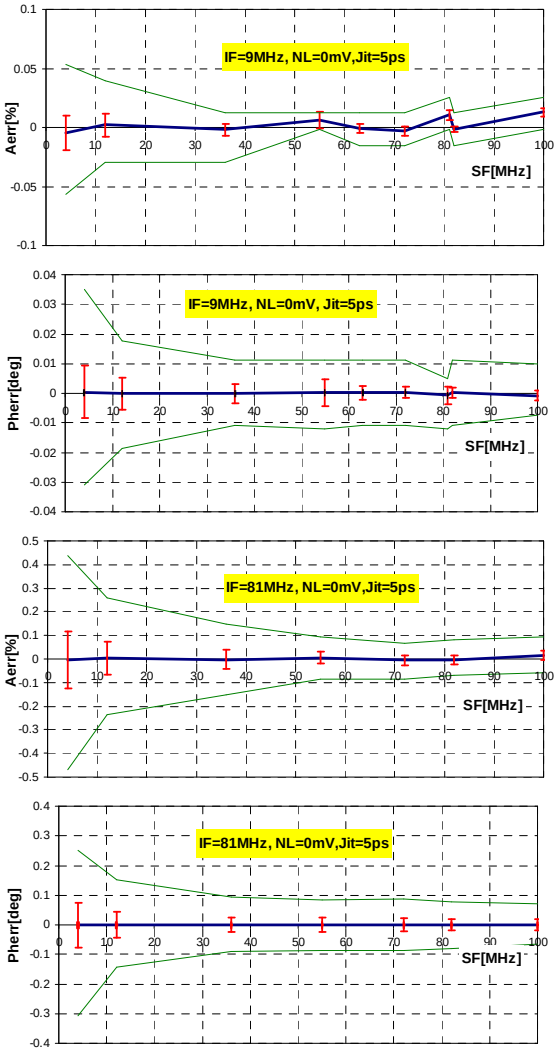

Fig. 5. Characteristics of amplitude and phase error for chosen parameters. Solid line – mean value of error, error bars – standard deviation, envelope – maximum error

The accuracy of IQ estimation in the presence of noise and clock jitters with ADC SNR degradation included. As can be noticed from Fig. 5 the estimation error decreases with sampling rate. Unfortunately the ADC parameters also degrades outside the nominal region. The AD6645 parameters SNR (Signal to Noise Ratio) and SINAD (Signal to Noise and Distortion) are not constant in the whole bandwidth. Therefore the SNR characteristics was modeled accordingly to technical specification and simulation of the whole system was done. The results of this simulation is presented in Fig. 6. The results of simulation show clearly that for the real noisy ADC there is an optimal sampling rate giving the best accuracy. For the AD6645 this optimal frequency is about 75MHz.

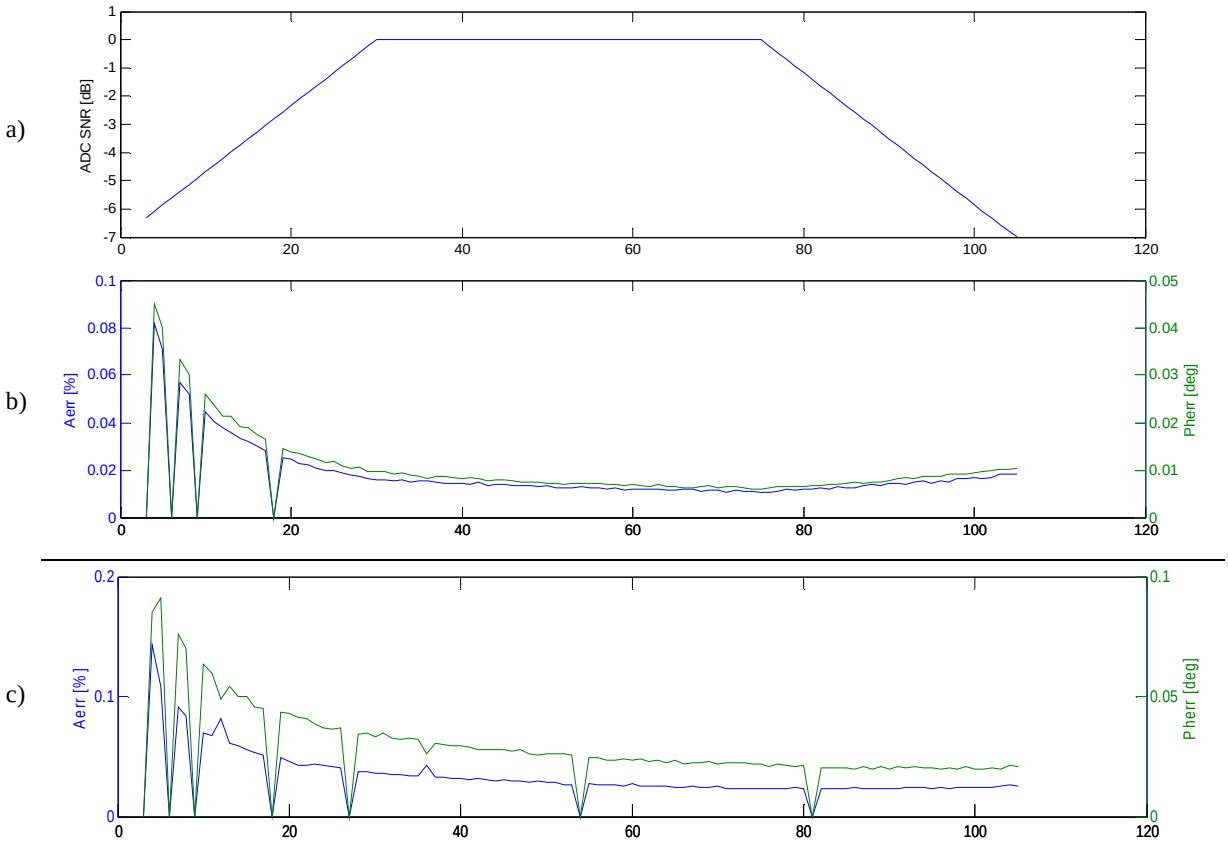

Fig. 6. Characteristics of amplitude and phase errors versus sampling rate for non-ideal ADC, noise level=0.5mV, jitters 5ps
a) the SNR model for AD6645 b) intermediate frequency = 9MHz c) intermediate frequency = 81MHz
(the drops of estimation error to zero means the "forbidden" sampling rate, not the exact estimation!)

TABLE 1. The amplitude estimation errors for various nonlinearity levels (IF=9MHz, SF-100MS/s)

INL	Aerr[%]	Aerr.std[%]	Aerrmin[%]	Aerrmax[%]
0	0.0161	0.0101	-0.0154	0.0532
1	0.0064	0.0093	-0.0291	0.0395
2	-0.0032	0.0101	-0.0291	0.0258
5	-0.0335	0.0089	-0.0702	-0.0016
10	-0.0854	0.0108	-0.1114	-0.0428
20	-0.1853	0.0105	-0.2211	-0.1525
50	-0.4875	0.0105	-0.5228	-0.4543
100	-0.9918	0.0082	-1.0303	-0.9617
200	-2.0022	0.0102	-2.0316	-1.9767

TABLE 2. The phase estimation errors for various nonlinearity levels (IF=9MHz, SF-100MS/s)

INL	Aerr[%]	Aerr.std[%]	Aerrmin[%]	Aerrmax[%]
0	0	0.0054	-0.0185	0.0208
1	-0.0002	0.0055	-0.0217	0.0208
2	0.0001	0.0055	-0.0217	0.0176
5	0	0.0056	-0.0201	0.0207
10	0	0.0054	-0.0217	0.0191
20	0.0001	0.0055	-0.0187	0.0158
50	-0.0001	0.0055	-0.0206	0.0216
100	-0.0001	0.0055	-0.0165	0.0177
200	-0.0001	0.0055	-0.0176	0.0194

The accuracy of IQ estimation in the presence of noise and clock jitters, with ADC and downconverter nonlinearity and with ADC SNR degradation included. The real ADC has nonlinear characteristics, the same concerns downconverter that is nonlinear by definition (it has to multiply the input signals). The nonliniearities of the whole system were gathered together for the simulation purpose and included in nonlinear characteristic of ADC. The nonlinearity was measured as the deviation in 1 LSB units of the transfer function of downconverter/ADC from a reference line. The tables 1 and 2 shows the numerical parameters of I and Q estimation accuracy for several nonlinearity factors. The results shows interesting features of proposed IQ estimator. The nonlinearity of the ADC and downconverter results mostly in disturbances of the amplitude of the signal, phase is practically not influenced by the nonlinearities. However the nonlinearity influences the estimation starting from the high level point. For typical ADCs integral nonlinearity is of order of single LSB or even below [6].

CONCLUSIONS

The IQ vector is an easy to use representation of sinusoidal signals. It allows to perform various operations on signal (addition two signals, multiplication by scalar, phase shifting). The I and Q components can be estimated from the series of digital samples of the

signal using simple VHDL module. The accuracy of the estimation depends on intermediate frequency, sampling rate and properties of ADC. For the given application those parameters can be optimized in order to obtain best accuracy. For the EU-XFEL, taking into account the accuracy of IQ estimation, the optimal intermediate frequency should be 9MHz or even lower. In this case the sampling rate 72MHz is optimal and easy to synthesize from Master Oscillator frequencies. However other elements (e.g. the requirements for downconverter filters) can limit the choice for optimal frequencies. It should be mentioned that LLRF system not only downconverts the RF signal but also upconverts I and Q output signals in modulator (Fig.1). The intermediate frequencies for downconversion and upconversion process do not need be the same, however if they are the same the whole system has more uniform design.

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APPENDIX

The set of equations (6) has to be solved using LSM. That leads to finding minimum of function f (eq. A).

$$f(I,Q)=\sum_{i=0}^{N-1}\left(x_i - a_i I - b_i Q\right)^2 \qquad \text{(A)}$$

where:

$$a_i = \sin(i\alpha)$$
$$b_i = \cos(i\alpha)$$

The unknown I and Q must yield zero first derivatives therefore:

$$\begin{aligned} I\sum_i a_i^2 + Q\sum_i a_i b_i - \sum_i a_i x_i = 0 \\ I\sum_i a_i b_i + Q\sum_i b_i^2 - \sum_i b_i x_i = 0 \end{aligned} \qquad \text{(B)}$$

what can be written in the form (C):

$$\begin{aligned} p_{11} I + p_{12} Q = s_1 \\ p_{12} I + p_{22} Q = s_2 \end{aligned} \qquad \text{(C)}$$

where:

$$p_{11} = \sum_{i=0}^{N-1}\sin^2(i\alpha), \qquad p_{22} = \sum_{i=0}^{N-1}\cos^2(i\alpha)$$

$$p_{12} = p_{21} = \sum_{i=0}^{N-1}\sin(i\alpha)\cos(i\alpha)$$

$$s_1 = \sum_{i=0}^{N-1} x_i \sin(i\alpha), \qquad s_2 = \sum_{i=0}^{N-1} x_i \cos(i\alpha)$$

One should note that p_{ij} are constant for chosen sampling scheme and s_i needs calculation.

However if the $N\alpha$ is an integer multiplicity of 2π the equations for p_{ij} can be simplified significantly. Fortunately such condition occurs in reality when the sampling rate is synchronized with intermediate frequency ($M \cdot IF = N \cdot SF$). In this case (D) expressions are valid:

$$\begin{aligned} p_{12} = p_{21} = \sum_{i=0}^{N-1}\sin(i\alpha)\cos(i\alpha) = 0 \\ p_{11} = \sum_{i=0}^{N-1}\sin^2(i\alpha) = p_{22} = \sum_{i=0}^{N-1}\cos^2(i\alpha) = \frac{N}{2} \end{aligned} \qquad \text{(D)}$$

Therefore the I and Q can be calculated from eq. (6)

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