Overview on the LLRF and MicroTCA developments at DESY

H. Schlarb

on behalf of the

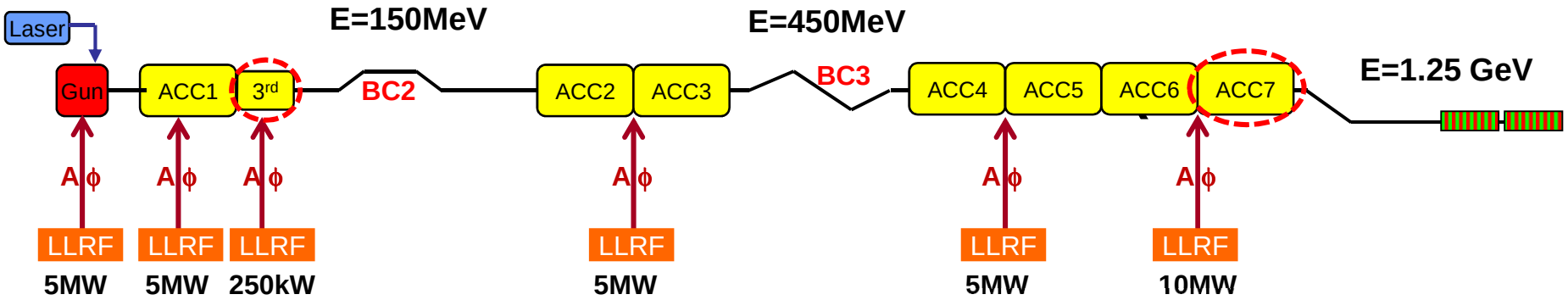
DESY LLRF Team

Outline:

- Developments 2011 – today
- Future requirements
- Modifications 1st → 2nd MTCA.4 Modules
- MTCA.4 boost through Helmholtz Validation Fund

HELMHOLTZ | GEMEINSCHAFT

Status at LLRF2011 conference:



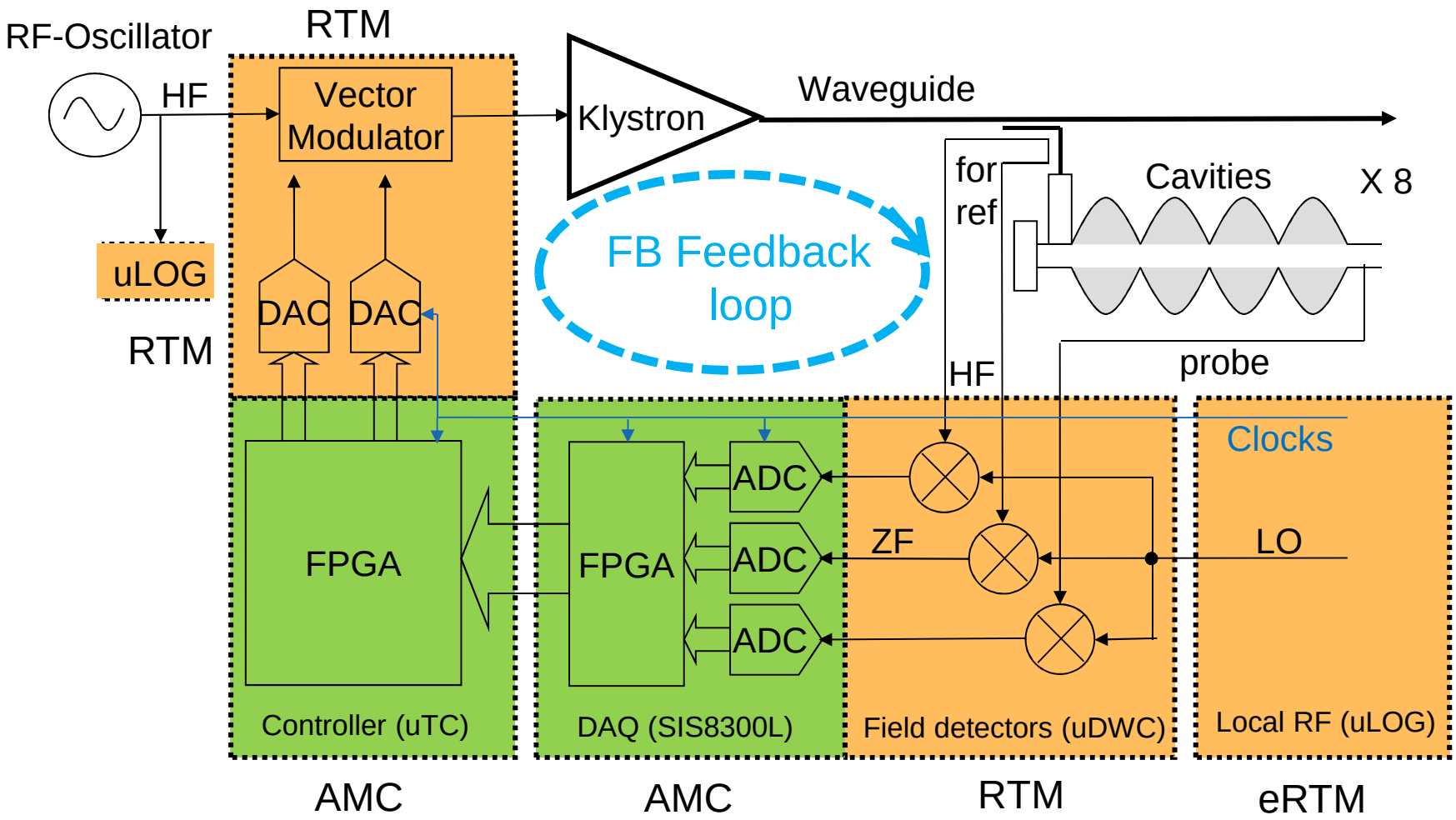
Station	until 2009	After upgrade 09/2010	Upgrade ~~06/2012~~ → 09/2013
RF gun	Simcon3.1	SimconDSP	uTCA (54MHz)
ACC1	SimconDSP (250kHz)	SimconDSP (250kHz)	uTCA (54MHz) @ acc. Module
ACC39	-	SimconDSP (54MHz)	uTCA (54MHz) @ acc. module
ACC23	DSP (250kHz)	SimconDSP (250kHz)	uTCA (54MHz) @ acc. module
ACC45	DSP/ATCA (250kHz/54MHz)	SimconDSP (250kHz)	uTCA (54MHz) (12/2012)
ACC67	DSP (250kHz)	SimconDSP (250kHz)	uTCA (54MHz)

Unified Hardware & Software

XFEL Hardware & Software

Work accomplished 2011-2013

> System overview



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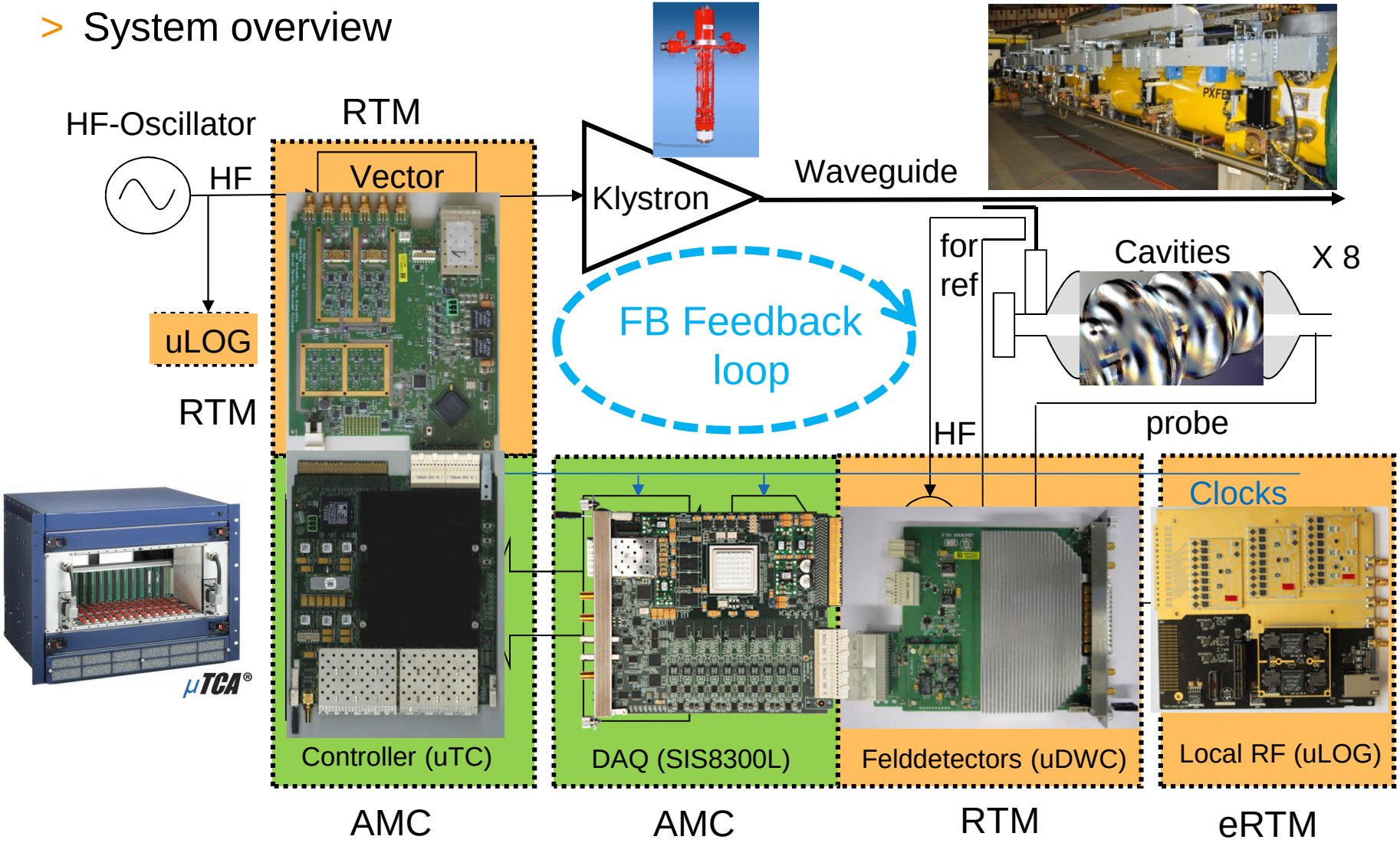
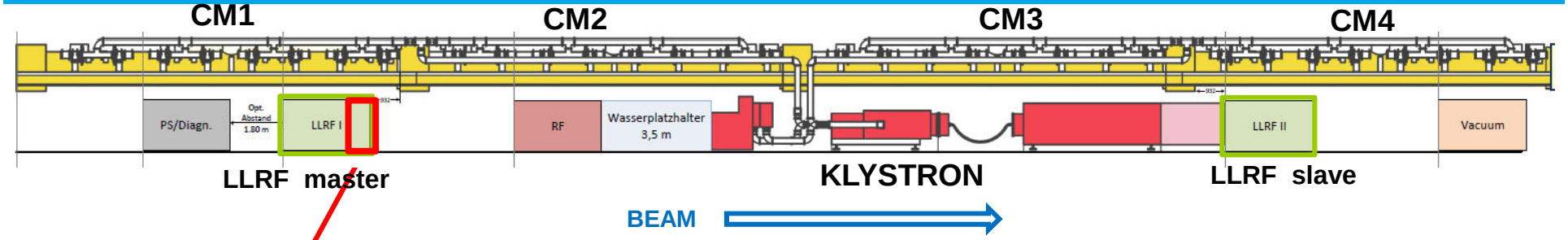
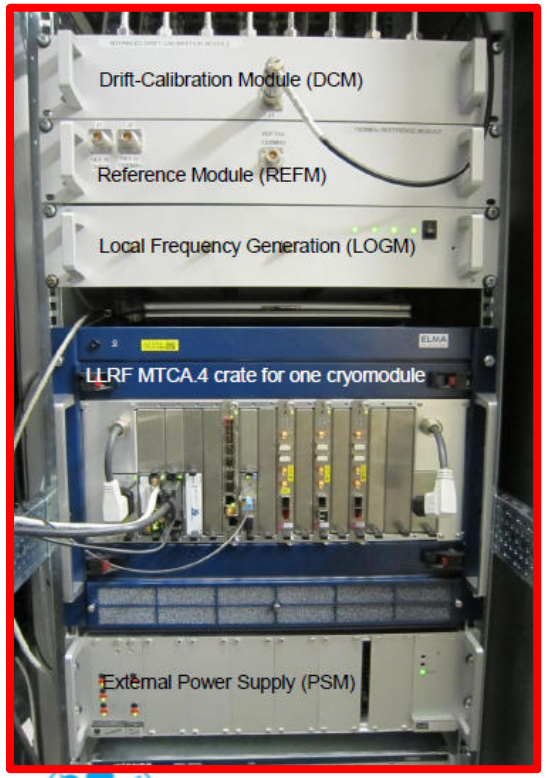
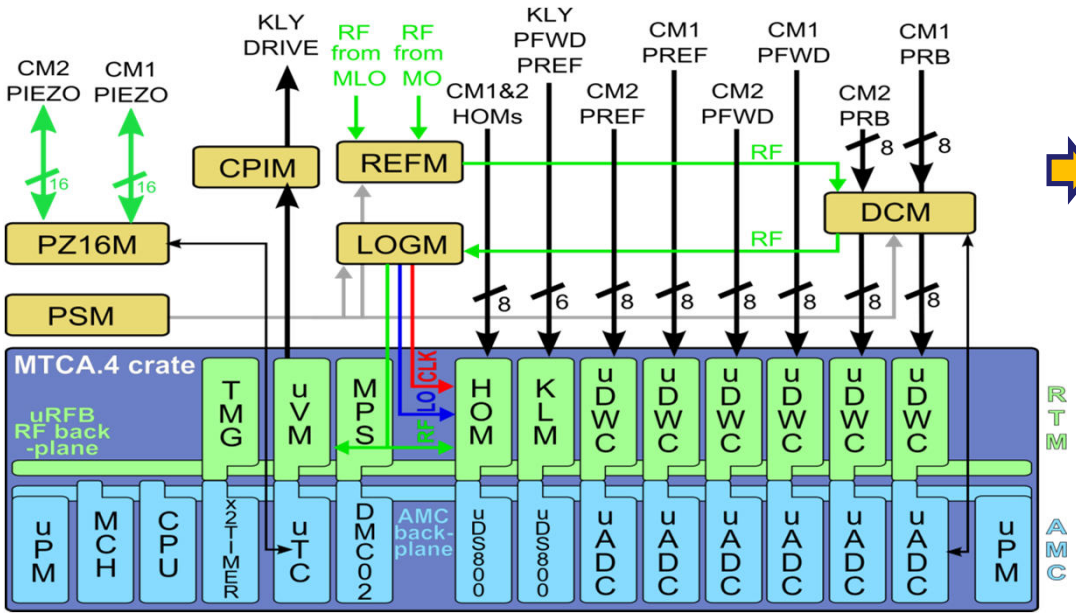


Work accomplished 2011-2013: XFEL LLRF System



< 28U Rack





Talk: J. Branlard

- MTCA.4 incl. complete sweet: LLRF/Diag./ Interlocks/HOM

Challenges:

- **Total: 27 RF station / 800 cavities / >3000 RF signals**
- **Stability requirements < 0.01% & 0.01deg**

Work accomplished 2011-2013: FLASH

- Infrastructure for new LLRF system installed
- XFEL style LLRF system commissioned
- Software Automation (mainly on VME-system):
  - Finite State Machine
  - Quench detection and interlocking
  - Automatic Piezo Tuning
  - Parameter optimization
  - High beam load operation
  - Integration / Improvement Beam Based Feedback
  - Large data acquisition system (DAQ)
- Migration to new system ongoing
- Effects due to radiation (SEU)

Talk: V. Ayvazyan

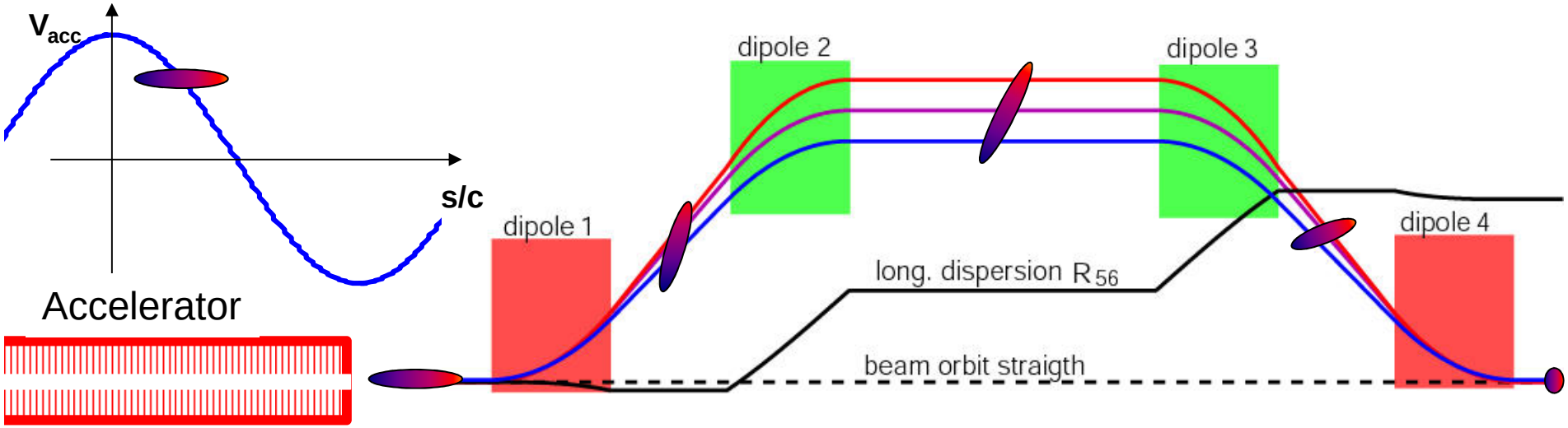
RF Gun, ACC1 & ACC39

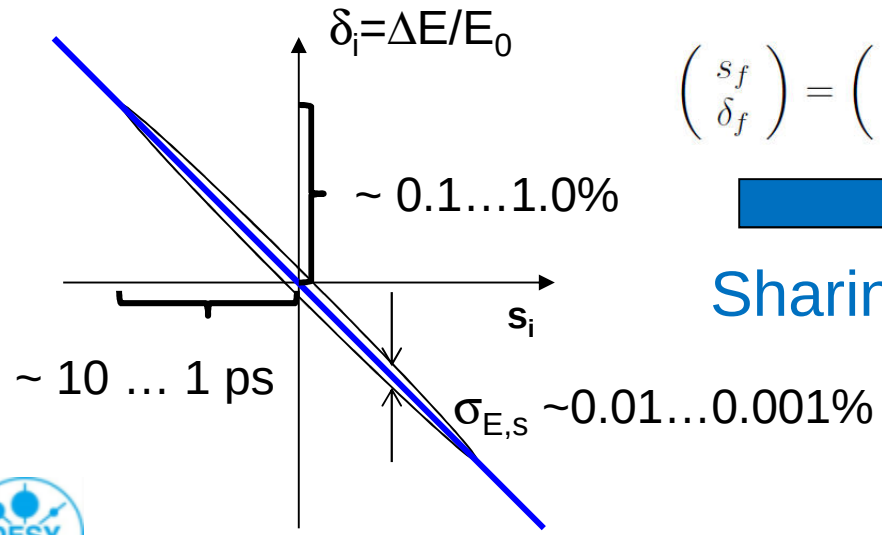
ACC23

ACC23, ACC45 and ACC67

Tolerances on RF stability: … what will be required?

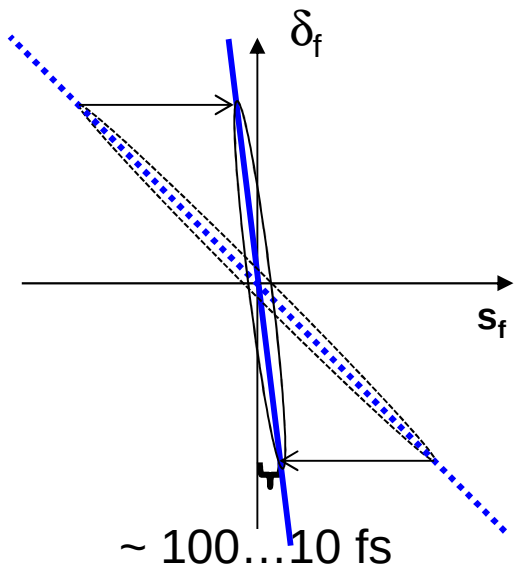
Energy chirp + energy dependent path length





$$\begin{pmatrix} s_f \\ \delta_f \end{pmatrix} = \begin{pmatrix} 1 & -R_{56} \\ 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} s_i \\ \delta_i \end{pmatrix}$$

Sharing process



Tolerances on RF stability: … what will be required?

> **Impacts the peak current** / longitudinal beam profile

> **Arrival time jitter:**

Tolerances on RF stability: … what will be required?

> **Impacts the peak current** / longitudinal beam profile

If $E_0 << E_1$ and $E_0' << E_1'$

6…3.5 ..4

$$\frac{\delta C}{C_1} = -(C_1 - 1)\left[\left(3\tan(\phi_1) + \frac{1}{\tan(\phi_1)}\right)(\delta\phi_1 - \omega_{RF}\delta t_{ini}) + 4\frac{\delta V_1}{V_1}\right]$$

Tolerance ∝ Compression

Phase & arrival

Amplitude

> **Arrival time jitter:**

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Tolerance ∝ Compression

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Example: C=100, dI/I<10% ⇒ $\phi \approx 0.014°$ and dV/V ≈ 2.5e-4
⇒ **multi-staged compression, but this adds cost**

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Tolerance ∝ Compression — **Phase & arrival** — **Amplitude**

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Amplitude — **Phase** — **Arrival**

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Amplitude **Phase** **Arrival**

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Amplitude — **Phase** — **Arrival**

> **Evolution:**

1990 Colliders	1°	&	1%	for phase / voltage
2000 FEL early	0.1°	&	0.1%	
2010 FEL now	0.01°	&	0.01%	
2020 FEL future	0.001°	&	0.001%	

since it scales with final bunch duration → < 1fs requested

Future requirements on XFEL LLRF System

> **Careful evaluation of current system limitations**

- Phase and amplitude stability
- Vector sum scaling and limitation of calibration techniques
- Analog and digital options and sufficient headroom in terms of resources
- System integration, beam based feedbacks and operation flexibility

⇒ t.b.d. **upgrade measures**

> **… to be prepared for future operation …**

- Achieve significant better than original XFEL specs. of 0.01deg/0.01% → 1mdeg/1e-3%
- Increase of macro-pulse repetition rates 10Hz → 25 Hz
- Beam energy stability of $\Delta E/E \sim$ 1e-6 at exit of linac
- Qualify Hardware for CW operation

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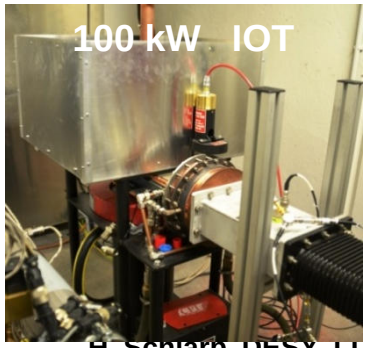
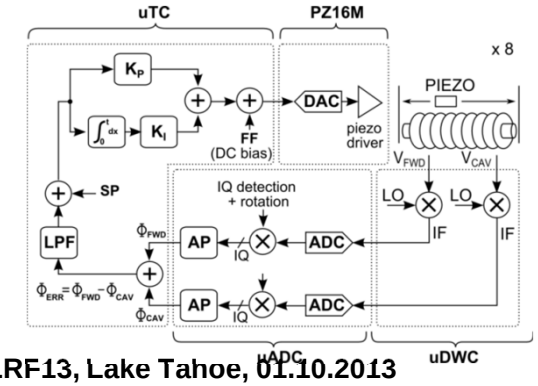
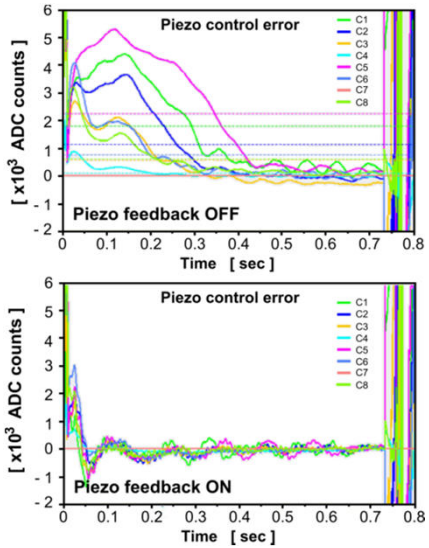
- Qualify Hardware for CW operation

First investigations of CW operation with XFEL modules at **CMTB**

Poster W. Cichalewski





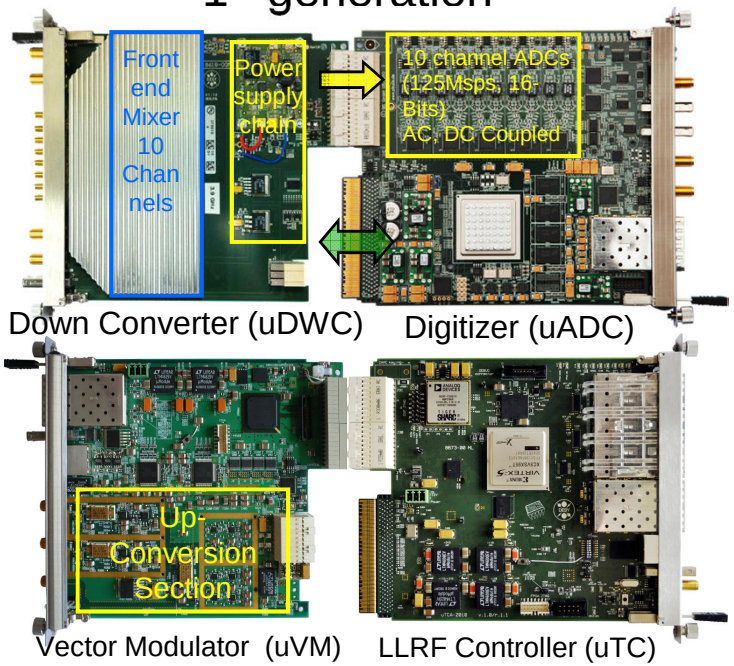


1st to 2nd generation MTCA.4 modules

> Core modules:

- Down converter 1.3GHz → IF=54Mhz
- SIS8300 10ch, 16bit, 125 MSPS
- Controller V5 based
- Vector modulator, 2 channel

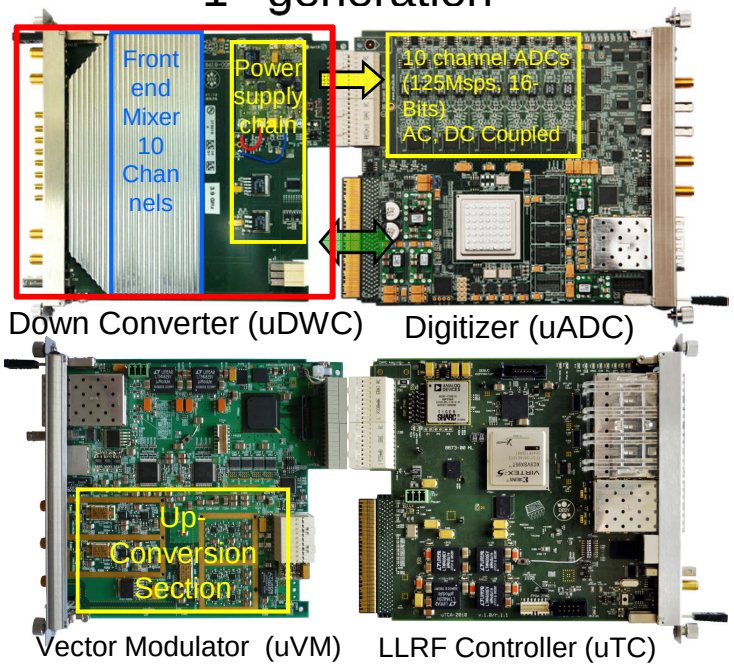
1st generation

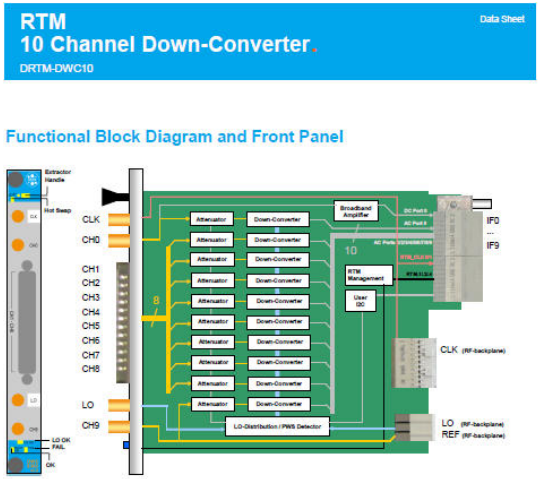


1st to 2nd generation MTCA.4 modules

- Core modules:
  - Down converter 1.3GHz → IF=54Mhz
  - SIS8300 10ch, 16bit, 125 MSPS
  - Controller V5 based
  - Vector modulator, 2 channel
- Developments DWC:
  - Switchable attenuators
  - Low return loss at connector
  - RF/clocks from RF Backplane
  - Licensed to industry

1st generation





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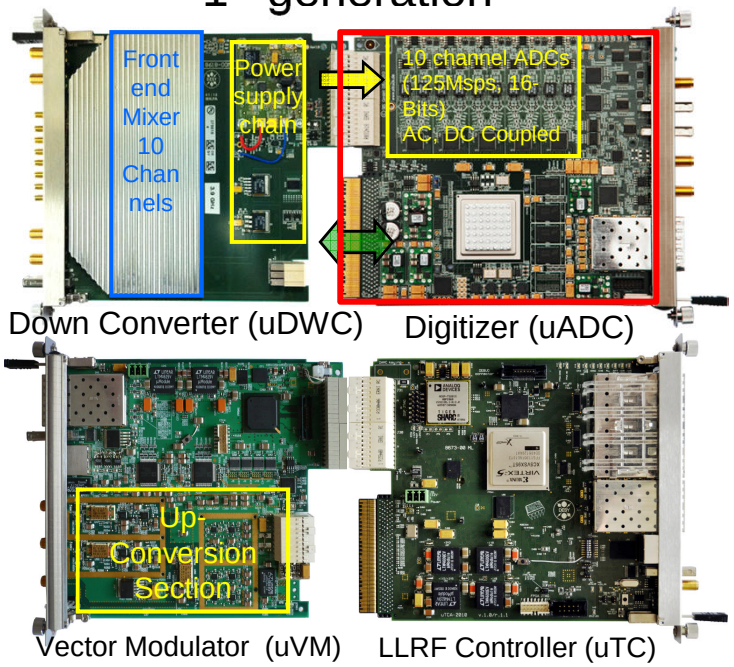
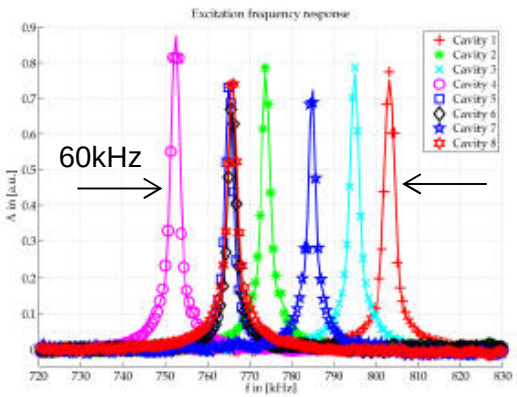
- Core modules:
  - Down converter 1.3GHz → IF=54Mhz
  - SIS8300 10ch, 16bit, 125 MSPS
  - Controller V5 based
  - Vector modulator, 2 channel
- Digitizer ⇒ SIS8300L
  - Resource limitation & communication limitation

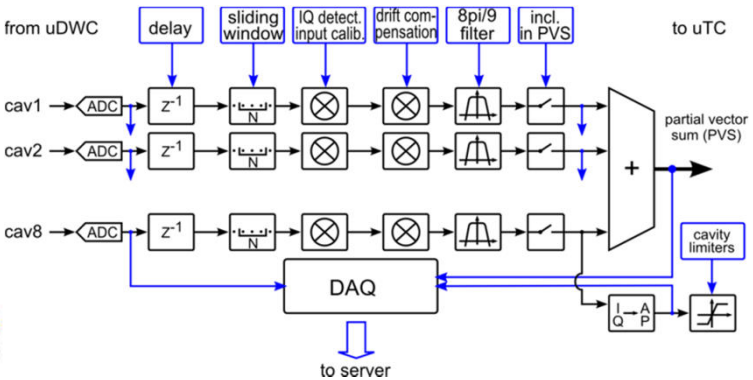
    → XC6VLX130T-2FFG1156C

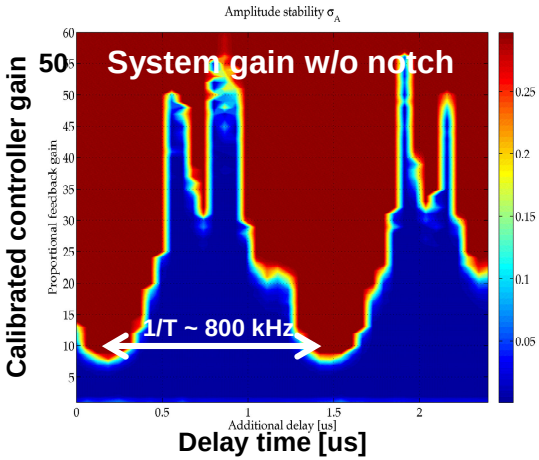
    → 6.6 Gbps transfer rate to controller

1st generation









1st to 2nd generation MTCA.4 modules

- Core modules:
  - Down converter 1.3GHz → IF=54Mhz
  - SIS8300 10ch, 16bit, 125 MSPS
  - Controller V5 based
  - Vector modulator, 2 channel
- Digitizer ⇒ SIS8300L
  - Resource limitation & communication limitation

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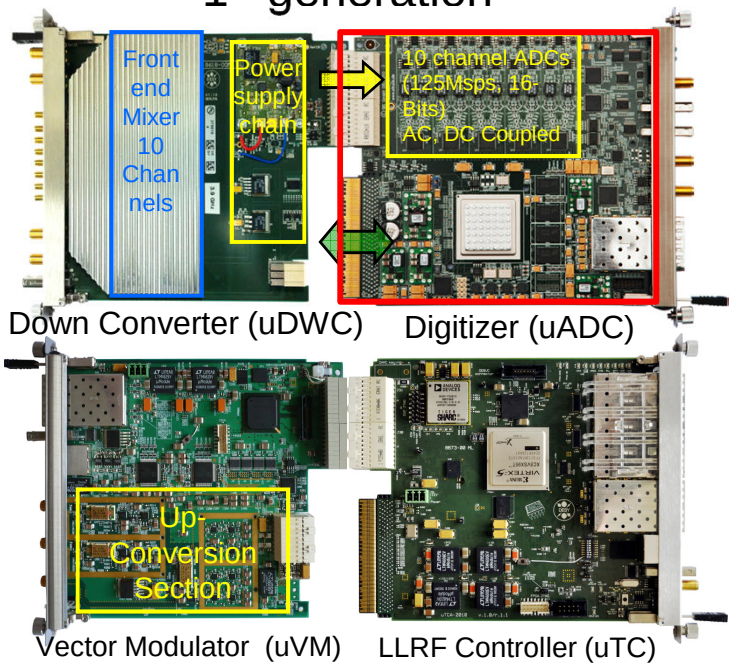
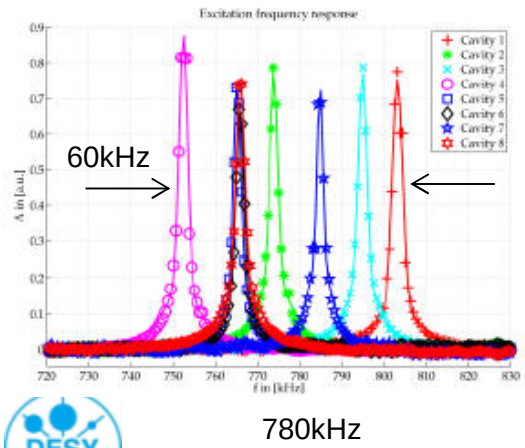
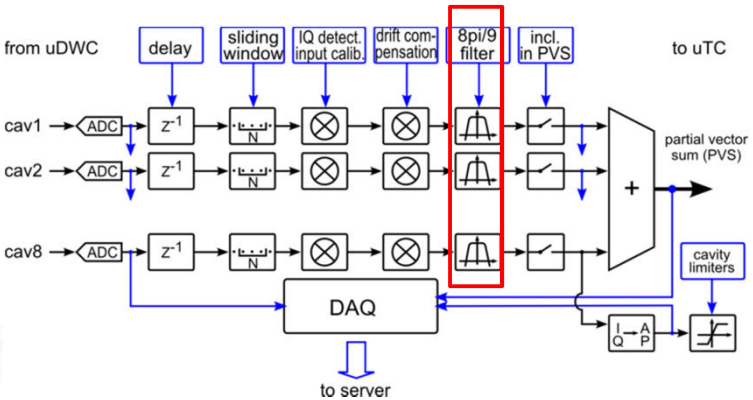
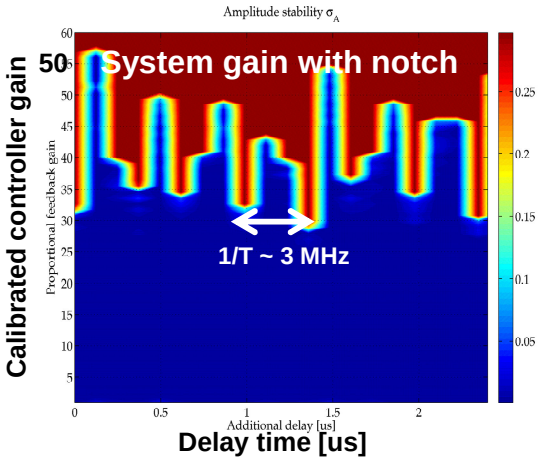






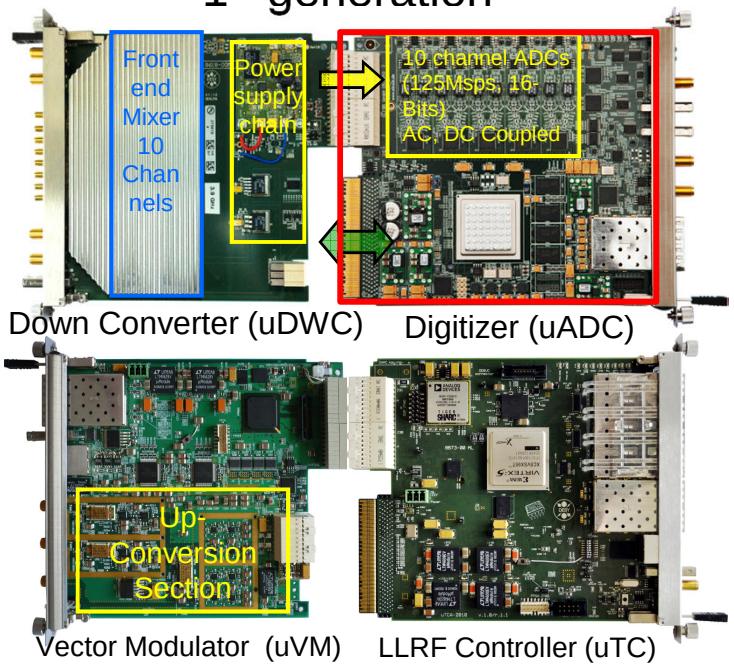


1st to 2nd generation MTCA.4 modules

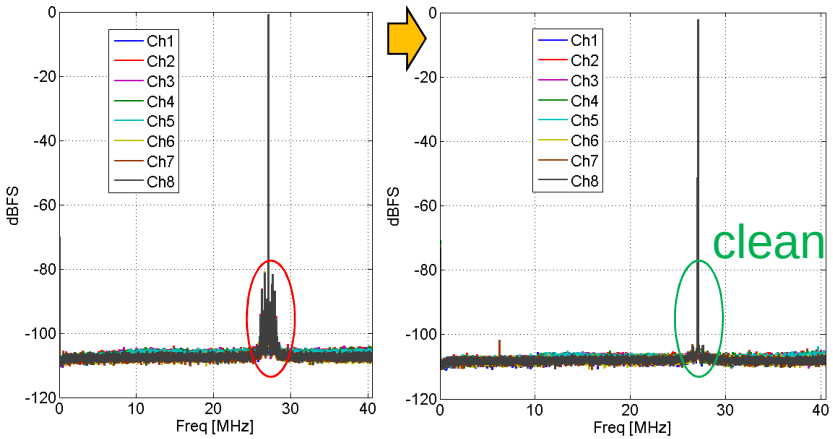
- Core modules:
  - Down converter 1.3GHz → IF=54Mhz
  - SIS8300 10ch, 16bit, 125 MSPS
  - Controller V5 based
  - Vector modulator, 2 channel
- Digitizer ⇒ SIS8300L
  - Resource limitation & communication limitation

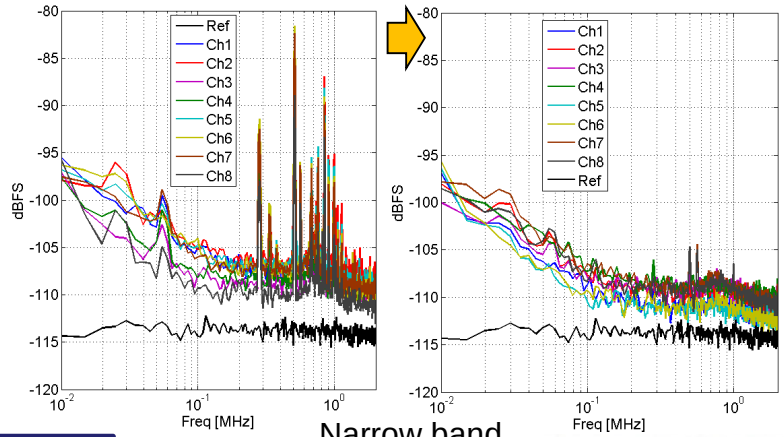
    → improved noise performance

1st generation



HW revision through HVF





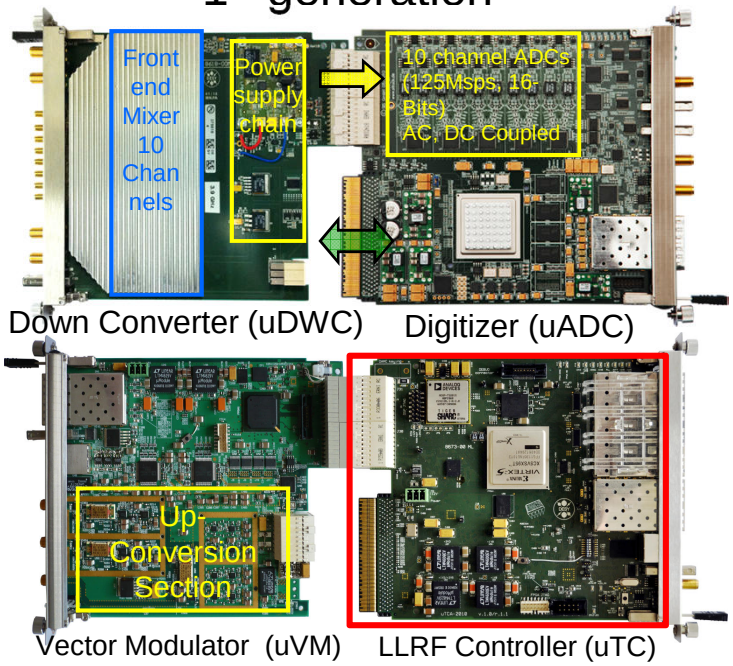
Narrow band

Poster: U. Mavric

1st to 2nd generation MTCA.4 modules

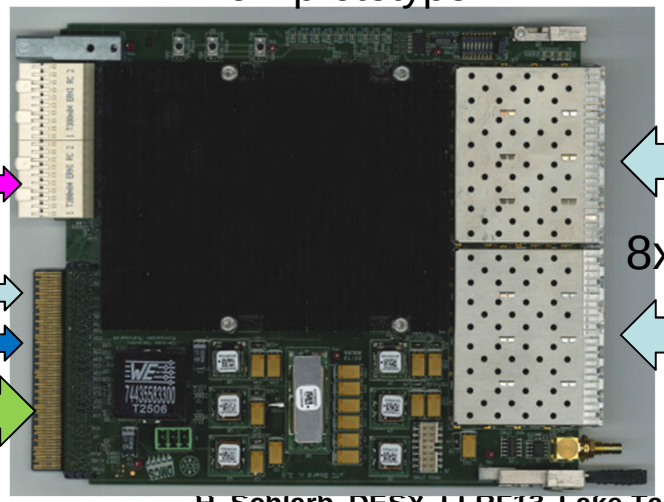
- Core modules:
  - Down converter 1.3GHz → IF=54Mhz
  - SIS8300 10ch, 16bit, 125 MSPS
  - Controller V5 based
  - Vector modulator, 2 channel
- LLRF controller => Kintex7 (K355/K420)
  - Communication speed (6.6G)/resources(x10)
  - Close to be licensed to industry

1st generation



General purpose module

New prototype



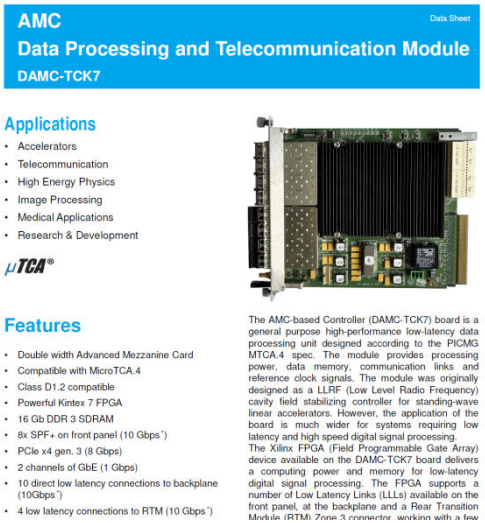
4x LLL(10Gbps)

2x GbE/SATA

4x PCIe gen 3

8x LLL(10Gbps)

8xSFP+



AMC

Data Sheet

Data Processing and Telecommunication Module

DAMC-TCK7

Applications

- Accelerators
- Telecommunication
- High Energy Physics
- Image Processing
- Medical Applications
- Research & Development

µTCA®

Features

- Double width Advanced Mezzanine Card
- Compatible with MicroTCA.4
- Class D1.2 compatible
- Powerful Kintex 7 FPGA
- 16 Gb DDR 3 SDRAM
- 8x SPF+ on front panel (10 Gbps*)
- PCIe x4 gen. 3 (8 Gbps)
- 2 channels of GbE (1 Gbps)
- 10 direct low latency connections to backplane (10Gbps*)
- 4 low latency connections to RTM (10 Gbps*)

The AMC-based Controller (DAMC-TCK7) board is a general purpose high-performance low-latency data processing unit designed according to the PICMG MTCA.4 spec. The module provides processing power, data memory, communication links and reference clock signals. The module was originally designed as a LLRF (Low Level Radio Frequency) cavity field stabilizing controller for standing-wave linear accelerators. However, the application of the board is much wider for systems requiring low latency and high speed digital signal processing.
The Xilinx FPGA (Field Programmable Gate Array) device available on the DAMC-TCK7 board delivers a computing power and memory for low-latency digital signal processing. The FPGA supports a number of Low Latency Links (LLLs) available on the front panel, at the backplane and a Rear Transition Module (RTM) Zone 3 connector, working with a few

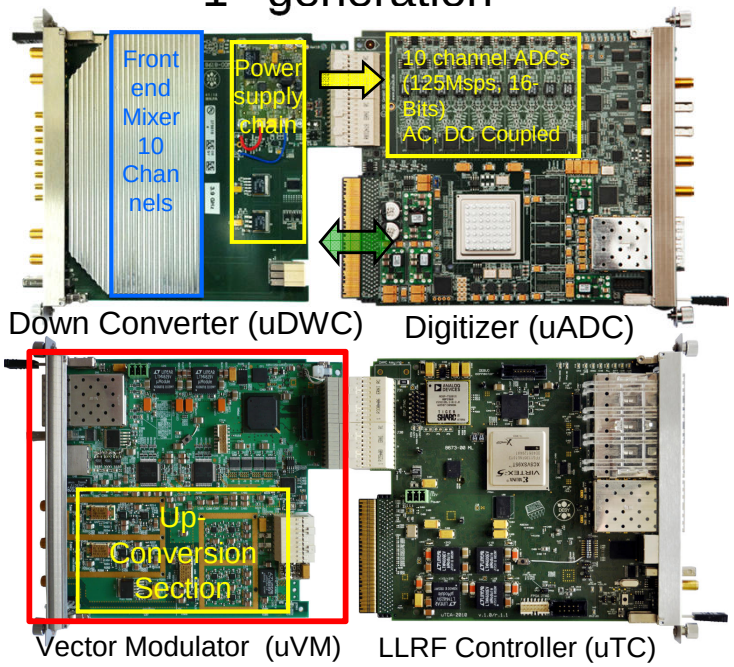
FT

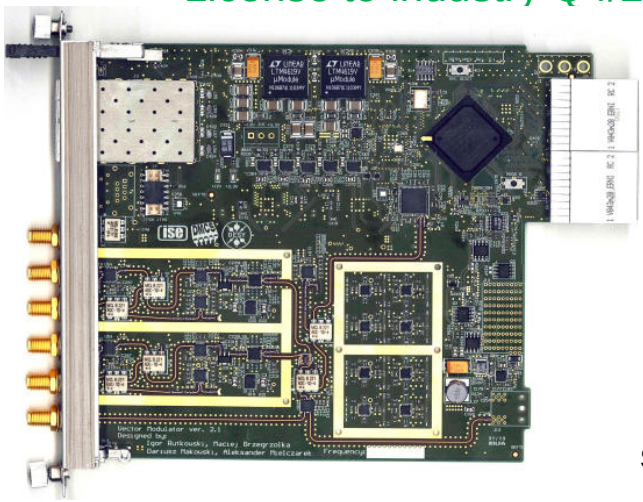
1st to 2nd generation MTCA.4 modules

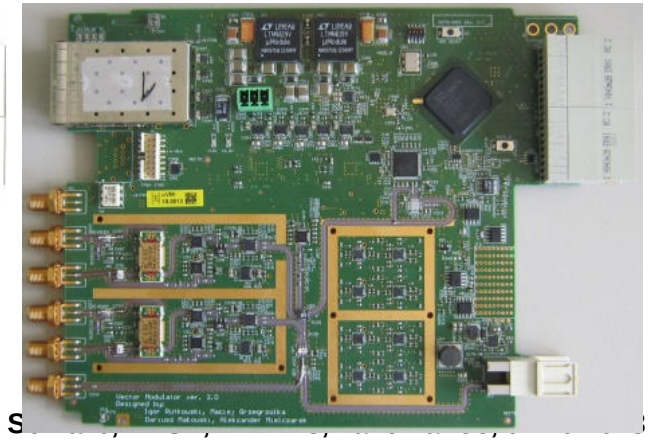
- Core modules:
  - Down converter 1.3GHz → IF=54Mhz
  - SIS8300 10ch, 16bit, 125 MSPS
  - Controller V5 based
  - Vector modulator, 2 channel
- Dual channel Up-conversion
  - Extended frequency range

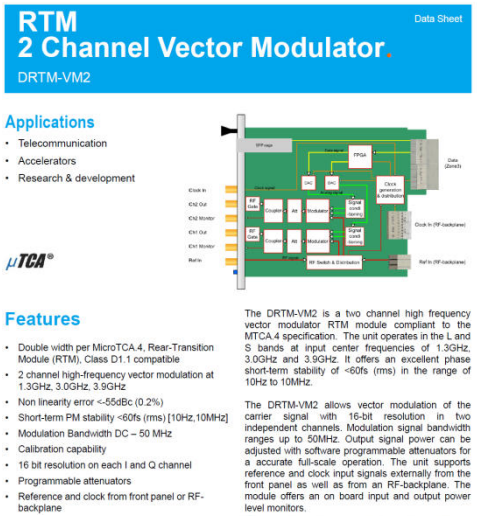
    LF (100MHz-2GHz), HF (2GHz-6GHz)
  - Improved noise floor (4-5 dB better)
  - License to industry Q4/2013

1st generation









RTM
2 Channel Vector Modulator
Data Sheet
DRTM-VM2

Applications
- Telecommunication
- Accelerators
- Research & development

µTCA®

Features
- Double width per MicroTCA.4, Rear-Transition Module (RTM), Class D1.1 compatible
- 2 channel high-frequency vector modulation at 1.3GHz, 3.0GHz, 3.9GHz
- Non linearity error <-55dBc (0.2%)
- Short-term PM stability <60fs (rms) [10Hz,10MHz]
- Modulation Bandwidth DC – 50 MHz
- Calibration capability
- 16 bit resolution on each I and Q channel
- Programmable attenuators
- Reference and clock from front panel or RF-backplane

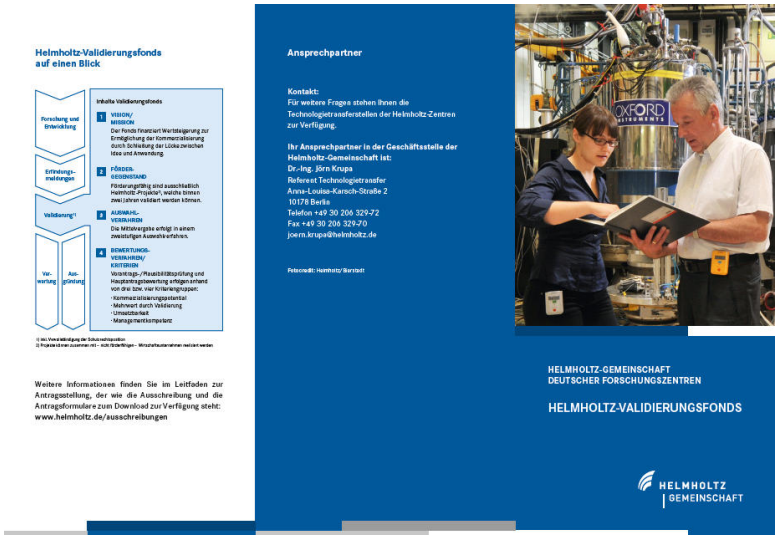
The DRTM-VM2 is a two channel high frequency vector modulator RTM module compliant to the MTCA.4 specification. The unit operates in the L and S bands at input center frequencies of 1.3GHz, 3.0GHz and 3.9GHz. It offers an excellent phase short-term stability of <60fs (rms) in the range of 10Hz to 10MHz.

The DRTM-VM2 allows vector modulation of the carrier signal with 16-bit resolution in two independent channels. Modulation signal bandwidth ranges up to 50MHz. Output signal power can be adjusted with software programmable attenuators for a accurate full-scale operation. The unit supports reference and clock input signals externally from the front panel as well as from an RF-backplane. The module offers an on board input and output power level monitors.

MTCA.4 boost though Helmholtz Validation Fund

HVF0016: “MTCA.4 for Industry”

- **Finance instrument to support the spin-off and technology transfer from scientific, technical inventions or developments from HGF centers to the industry and society**



Helmholtz-Validierungsfonds auf einen Blick

Inhalte Validierungsfonds

1 VISION/ MISSION
Der Fonds finanziert Wertsteigerung zur Ermöglichung der Kommerzialisierung durch Schließung der Lücke zwischen Idee und Anwendung

2 FÖRDER-GEGENSTAND
Fördergegenstand sind ausschließlich Helmholtz-Projekte[1], welche binnen zwei Jahren validiert werden können.

3 AUSWAHL-VERFAHREN
Die Mittelvergabe erfolgt in einem zweistufigen Auswahlverfahren.

4 BEWERTUNGS-VERFAHREN/ KRITERIEN
Vorabfragen/ Plausibilitätsprüfung und Hauptantragsbewertung erfolgen anhand von drei bzw. vier Kriterienkomplexen:
- Kommerzialisierungspotential
- Mehrwert durch Validierung
- Umsetzbarkeit
- Managementkompetenz

Forschung und Entwicklung
Erfindungs-meldungen
Validierung[1]
Ver-wertung
Aus-gründung

Weitere Informationen finden Sie im Leitfaden zur Antragsstellung, der wie die Ausschreibung und die Antragsformulare zum Download zur Verfügung steht: www.helmholtz.de/ausschreibungen

Ansprechpartner

Kontakt:
Für weitere Fragen stehen Ihnen die Technologietransferstellen der Helmholtz-Zentren zur Verfügung.

Ihr Ansprechpartner in der Geschäftsstelle der Helmholtz-Gemeinschaft ist:
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Fotocredit: Helmholtz/ Barnbeck

HELMHOLTZ-GEMEINSCHAFT DEUTSCHER FORSCHUNGSZENTREN

HELMHOLTZ-VALIDIERUNGSFONDS

HELMHOLTZ | GEMEINSCHAFT

Main objective: <u>Forster industrialization of MTCA.4 to industry</u> and its application research and science

Stimulus to rapidly overcome initial barriers of a new electronic crate standard…

Helmholtz validation-fond (HVF)

- **Starting point : Nov. 2011 release of MTCA.4 standard by PICMG**
  PICMG = PCI Industrial Computer Manufacturing Group(http://www.picmg.org)
- **July 2012 project start with industrial consortium with 3.9M€**

HELMHOLTZ ASSOCIATION — **50%**

DESY — **30%**

struck innovative systeme, ELMA, Schroff, AD-TE-C, N.A.T., TEWS TECHNOLOGIES, AMPEGON — **20%**

New partners: INTERFACE CONCEPT, powerBridge Computer, eicSys GmbH, COSYLAB

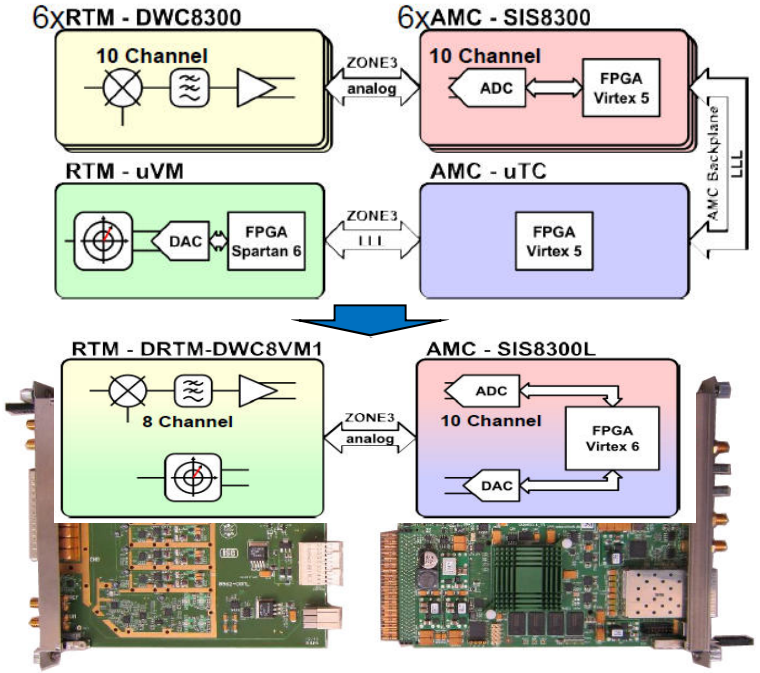
Negotiation Phase: CAEN, kontron, vadatech, Laurin AG

Helmholtz validation-fond (HVF)

AP1: RF control system in MTCA.4

AP1.1 Revision of existing modules

AP 1.1.1 Field Detection (uDWC)
AP 1.1.2 Controller (uTC)
AP 1.1.3 RF driver unit (uVM)
AP 1.1.4 Local RF-Generation (uLOG)



AP1.2 Cost opt. for Single Cavities Applications

AP 1.2.1 Field detector with RF driver (uDWC-VM)
AP 1.2.2 High-end Digitizer (DAQ-LNC)

Poster: M. Hoffmann

AP1.3 Extending Portfolio in Frequency

AP 1.3.1 Field detector with RF driver (uVM, 0.35-6GHz)
AP 1.3.2 Local RF-Generation (uLOG, 0.35-6GHz)
AP 1.3.3 RTM with local clock circuit (uCLK-RTM, 10–350MHz)
AP 1.3.4 Global clock generation (uCLK-eRTM, 10-350MHz)
AP 2.2.8 Backplane Development for 10 Gbit/sec Transfer Speed

AP1.4 Supplementary systems for RF control

AP 1.4.1 Multi-channel Direct RF-sampling (uDS800)
AP 1.4.2 AMC carrier with motor/RTM with Piezo driver (uFMC20)

Talk: S. Habib

AP1.5 Introduction of RTM-RF Backplane

AP 1.5.1 Development of RTM-RF Backplane concept
AP 1.5.2 Crate integrated RF source (uOSC_eRTM)

Poster: Konrad

Talk: K. Czuba

K. Czuba

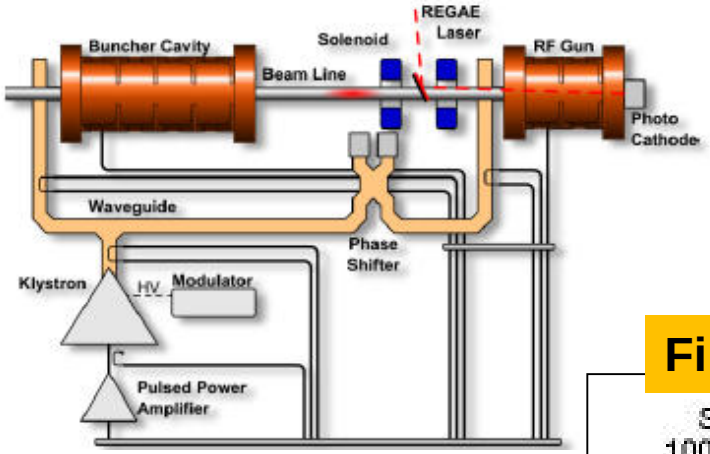
Due to modularity only moderate effort required to develop RF controls for

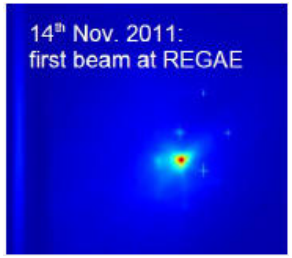
- **1/2/4/.. Cavities**
- **NRF/SRF**
- **10-6000 MHz**
- **valuable add on's**

GEMEINSCHAFT

First test of DWC8VM1 at REGAE@3.0GHz:

- **REGAE (Relativistic Electron Gun for Atomic Exploration) :**
  - Electron source for time resolved diffraction experiments

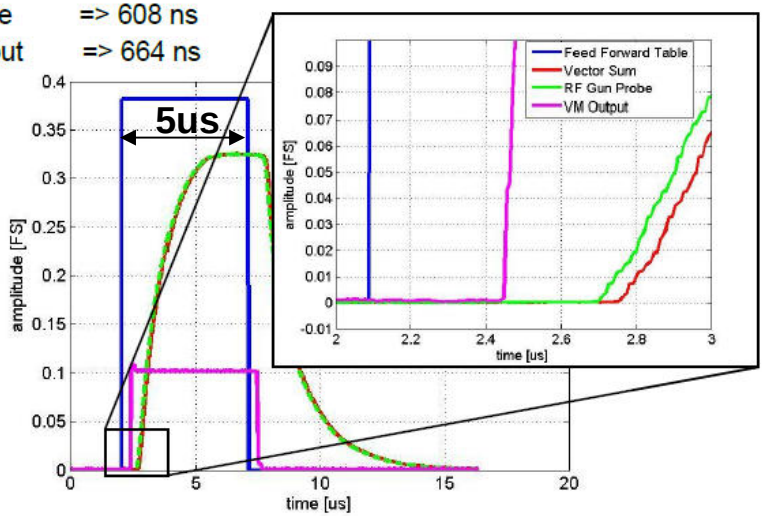




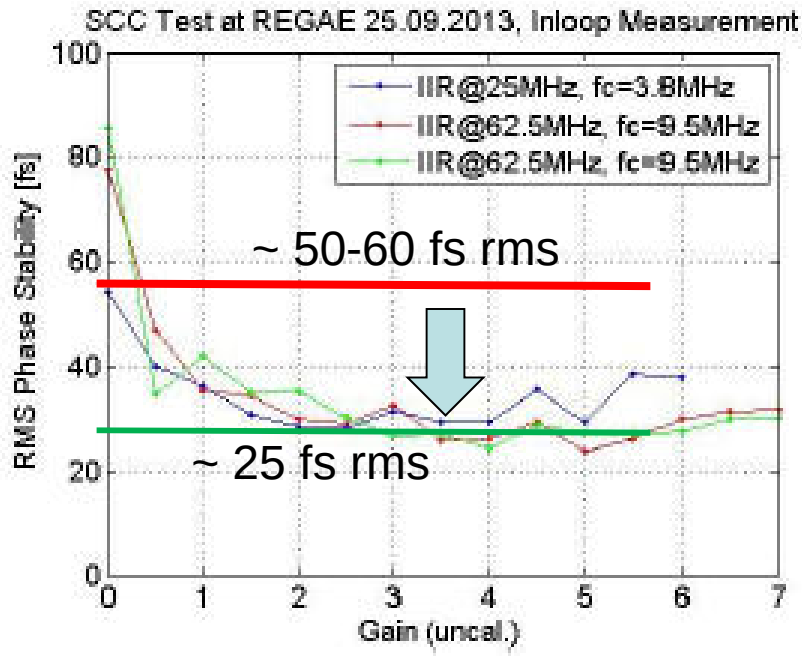
Poster: M. Hoffmann

Delay Budget (new System):

- Vector Mod. Output => 360 ns
- RF Gun Probe => 608 ns
- Controller Input => 664 ns



First test with RF intra-pulse FB



Supplementary modules for LLRF (AP1.4)

> Modules for RF controls

- Components: **Supplementary Modules (AP1.4)**

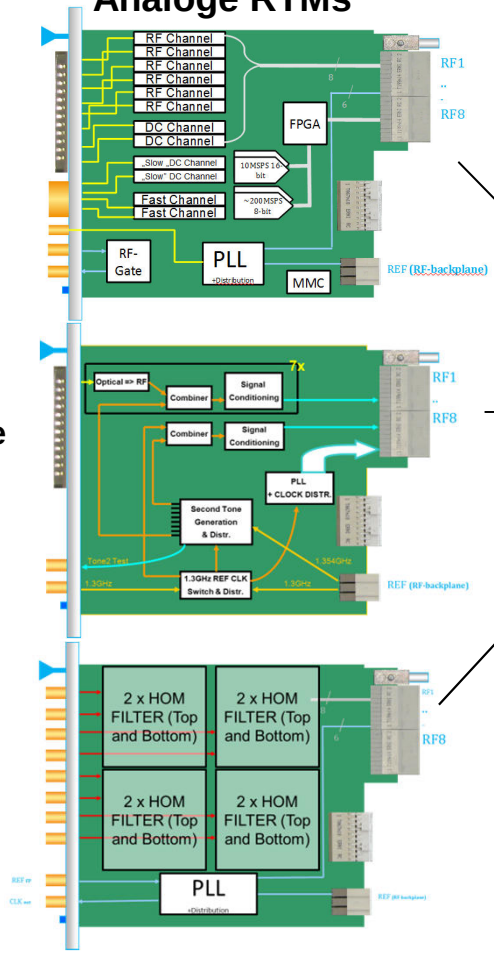
Application examples:

Klystron life-time Management

High-Order Mode measurements (1.3/1.7/2.4GHz)

Femtosecond Fiberoptic Synchronisation

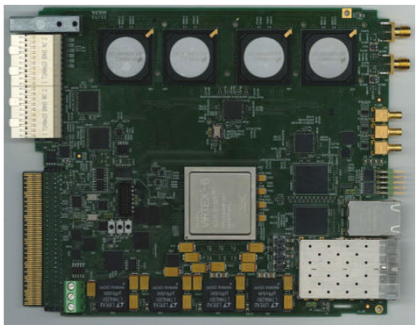
Analoge RTMs



AP1.4.1: uDS800

Prototype in Test

8 x 800MSPS, 12 bit.



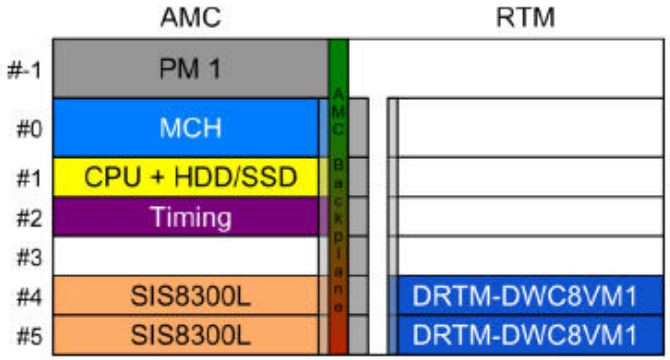
direct RF Sampling
Up to 2.7 GHz

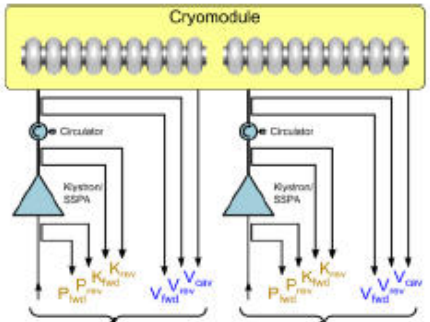
Very large Application spectrum

Several requests
ITER/Frankreich
INFN/Italien
KIT/Deutschland
Uni. of Hawaii

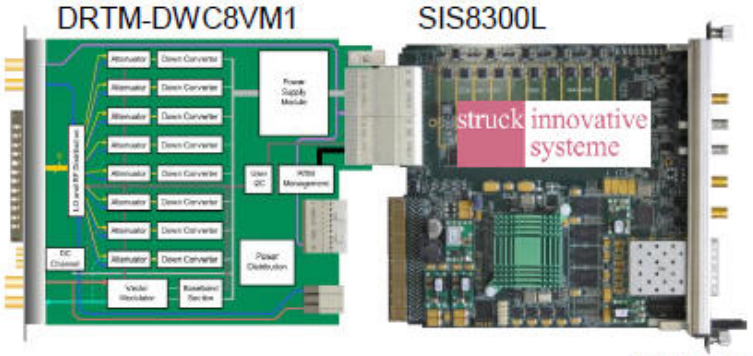
DAMC-DS800

Supplementary modules for LLRF – Fully integrated control for SRF cavities –

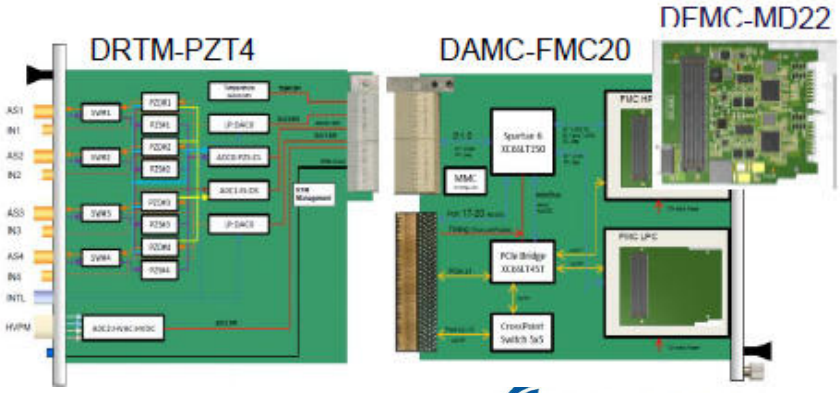




Similar system used for fs-laser synchronization

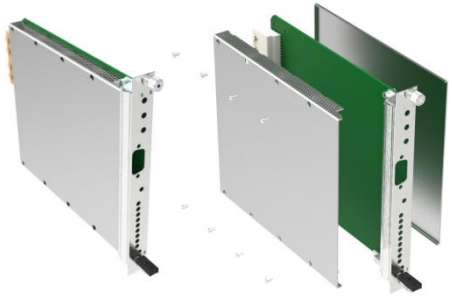


- **SIS8300L + DRTM-DWC8VM1**
  - LLRF field detection and controller
- **DAMC-FMC20 + DFMC-MD22 + DRTM-PZT4**
  - Piezo driver (PZT4) for cavity piezo tuner
  - Motor driver (MD22) for cavity frequency tuner
- **Free slot #3 for:**
  - Coupler interlock, diagnostic (BPM), fast klystron protection



Helmholtz validation-fond (HVF)

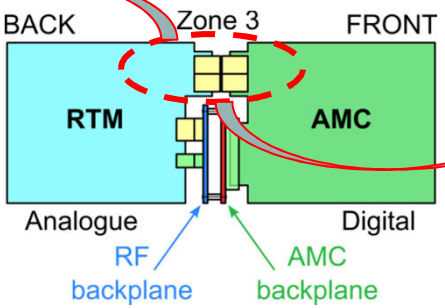
Further supporting working packages



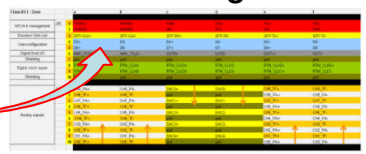
EMI Optimization und Classification of MTCA.4 components

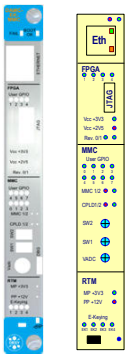
AP 2.2.1 ***EMI Test Boards***
AP 2.2.2 EMI Current and Noise Distribution within MTCA.4 Systems
AP 2.2.3 Optimizing of MTCA.4 Crate-contacts and grounding
AP 2.2.4 Manufacturing of AMC and RTM Shielding
AP 2.2.5 Development of EMI Bypass-Concept
AP 2.2.6 Minimizing der Vibration for Precision High Frequency References
AP 2.2.7 EMI Classification of AMC/RTM Modules
AP 2.2.8 Backplane Development for 10 Gbit/sec Transfer Speed

Module Management Controller / ZONE3 recommendations

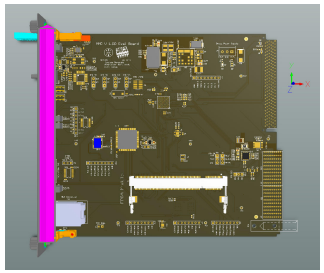


Pin assignment





MMC Starter Kit



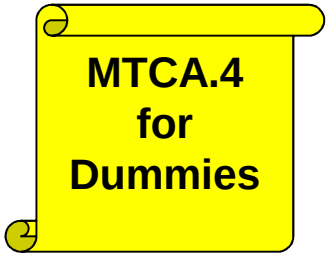
Support,

consulting

& annual workshop

MTCA Tutorial

Book to be published



Embeddedworld 2013 Nürnberg

IPAC 2013 Shanghai

Thanks for attention

URL http://mtca.desy.de/

Next workshop date:
11/12 Dec. 2013
Tutorial on 10. Dec