

CONSIDERATIONS FOR THE CHOICE OF THE INTERMEDIATE FREQUENCY AND SAMPLING RATE FOR DIGITAL RF CONTROL

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Abstract

Modern FPGA-based rf control systems employ digital field detectors where an intermediate frequency (IF) in the range of 10 to more than 100 MHz is sampled with a synchronized clock. Present ADC technology with 14-16 bit resolution allows for maximum sampling rates up to 250 MHz. While higher IF's increase the sensitivity to clock jitter, lower IF frequencies are more susceptible to electromagnetic noise. The choice of intermediate frequency and sampling rate (SR) should minimize the overall detector noise, provide high measurement bandwidth and low latency in field detection, and support algorithms for optimal field estimation.

INTRODUCTION

The choice of the IF frequency in analogue feedback systems is usually made with respect to a reasonable range of frequencies (typ. 10–100 MHz or direct conversion to baseband) while a specific frequency is based on the availability of components (such as 10 MHz or 70 MHz) including filters, mixers, directional couplers and others. In digital systems which employ digital downconversion (digital receiver algorithms where the field vector is calculated from the IF frequency samples) there exist much wider choice of frequencies. They can be chosen with an upper limit dictated by technological limitations including sampling rate and bit-resolution of the ADC [1] and stability of the synthesized clock in the case of digital downconversion. Criteria for the selection of clock and IF frequency include:

- Minimize measurements noise
 - with respect to signal conditioning
 - with respect to conversion noise
 - with respect to clock jitter
- Up-date rate, latency of measurement
- Stability of LO generation, clock and rf reference
 - Reference before and during pulse
- Linearity correction of downconverter
- IQ- detection algorithm
- Filtering of IF signal

GENERAL CONSIDERATION

Superconducting accelerators under construction or in planning require an accelerating phase stabilities ranging from 1 deg. down to 0.01 deg. and amplitude stabilities ranging from 1% to 0.01% at operating frequencies of the order of 1 GHz. This requires low noise field detection schemes with measurement bandwidth of the order of MHz. In digital control system the rf probe signal is

usually downconverted to an IF frequency of 10-100 MHz where signal conditioning and analogue to digital conversion takes place.

Since the IF frequency dictates also the LO frequency, care must be taken that the LO frequency is easy to generate so that low noise and low phase drift performance can be achieved. In the case of pulse accelerator where the rf pulse is preceded by a phase calibration reference pulse, only short term stability of the LO frequency is of importance. Another criteria for the choice of the IF and LO frequency is that this frequency should not be present in other systems so that leakage to the field detector cannot cause errors on the field measurement.

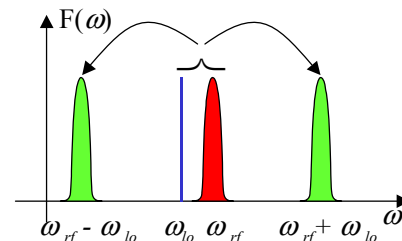


Fig. 1. Signal downconversion

The downconversion process can be performed by nonlinear mixers multiplying RF signal and reference signal (Fig. 1). This operation shifts frequency spectrum of the signal preserving unchanged information about amplitude and phase of RF field.

The IF signal contains the same amplitude $A_{rf}(t)$ and phase $\varphi_{rf}(t)$ information as the RF-signal, except for an amplitude scaling by constant and arbitrary but constant phase difference. The analogue IF signal $x(t)$ is sampled by ADC with constant sampling rate.

Direct IQ detection scheme

The I and Q components (In phase and in Quadrature) of IF signal can be numerically calculated from two successive signal samples (eq. 1).

$$I = \frac{x_1 \sin(\varphi + \Delta\varphi) - x_2 \sin \varphi}{\sin \Delta\varphi} \quad (1)$$

$$Q = -\frac{x_1 \cos(\varphi + \Delta\varphi) - x_2 \cos \varphi}{\sin \Delta\varphi}$$

where $\Delta\varphi$ is a phase advance between two consecutive samples, φ is related to an arbitrary chosen initial phase.

For hardware implementation of equations (1) four multipliers are needed. The samples of I and Q

components are obtained every signal sample with latency of one sampling period. However the DC offset in sampled input signal causes errors in I and Q computation, therefore this scheme requires offset cancellation by hardware or software (computation of DC level and correction of signal values – that requires additional adders and introduces additional latency).

IQ detection scheme with averaging for the integer number of IF periods

Other method of I and Q calculation averages signal samples during integer number of IF signal periods. The frequency of IF signal and sampling rate must therefore fulfill a condition $N \cdot IF = M \cdot SR$ (M, N – integer numbers). The N samples are taken during M periods of IF signal therefore latency is M/IF . I and Q can be calculated from (2) [2]:

$$I = \frac{2}{N} \sum_{i=0}^{N-1} x_i \sin(\varphi + i\Delta\varphi) \tag{2}$$

$$Q = \frac{2}{N} \sum_{i=0}^{N-1} x_i \cos(\varphi + i\Delta\varphi)$$

The hardware implementation of Eq.2 requires only 2 MAC (multiply and accumulate) units. It also automatically cancels constant offset and allows to scale and rotate the resulting vector in parallel to I and Q calculation. The averaging of the samples in Eq.2 reduces noise and jitter influence. The dependency of error on IF and SR for given noise and jitter level is presented in Fig.2. This method introduces more latency in comparison to method given in eq.1 (2 samples are needed) but if M and N numbers are carefully chosen the additional latency can be quite small. Several possible

frequencies combinations and resulting latency are presented in Fig. 3 for $1\text{MHz} < IF < 100\text{MHz}$ and $10\text{MSps} < SR < 105\text{MSps}$. All frequencies were assumed to be multiplication of 1MHz. The shortest latency of 29ns gives the combination of $IF=70\text{MHz}$ and $SR=105\text{MPps}$.

UP-DATE

The up-date rate of the measurement must be compatible with the up-dates of the actuator of the digital feedback. In the case of superconducting cavities up-date rates of a few MHz are sufficient for a unity gain of the controller of several hundred kHz. This results in up-date periods of 100–1000 ns. Assuming a sampling rate of the ADC of 100 MHz and use of 3 samples for the field vector measurement one would obtain 10 measurements in 300 ns, sufficient to fit a linear slope on the I and Q measurements and predict the field at time of actuator control.

MEASUREMENTS NOISE LEVEL

The measurement noise level of a 100 MHz, 14-bit ADC with input range of +1 Volt (into 50 Ohms) and 300 MHz bandwidth is typically of the order of 0.03% rms (-300 uV rms) of full scale (pk.). If driven with a bipolar sinusoidal IF signal at 50% of FS the expected phase and amplitude error from 2 samples is of the order of 0.06 degrees in phase and $1e-3$ in amplitude. Averaging over 50 measurements in 1 us will reduce the noise level to 0.01 deg. and $2e-4$ respectively which is sufficient for the most stringent requirements in superconducting accelerators.

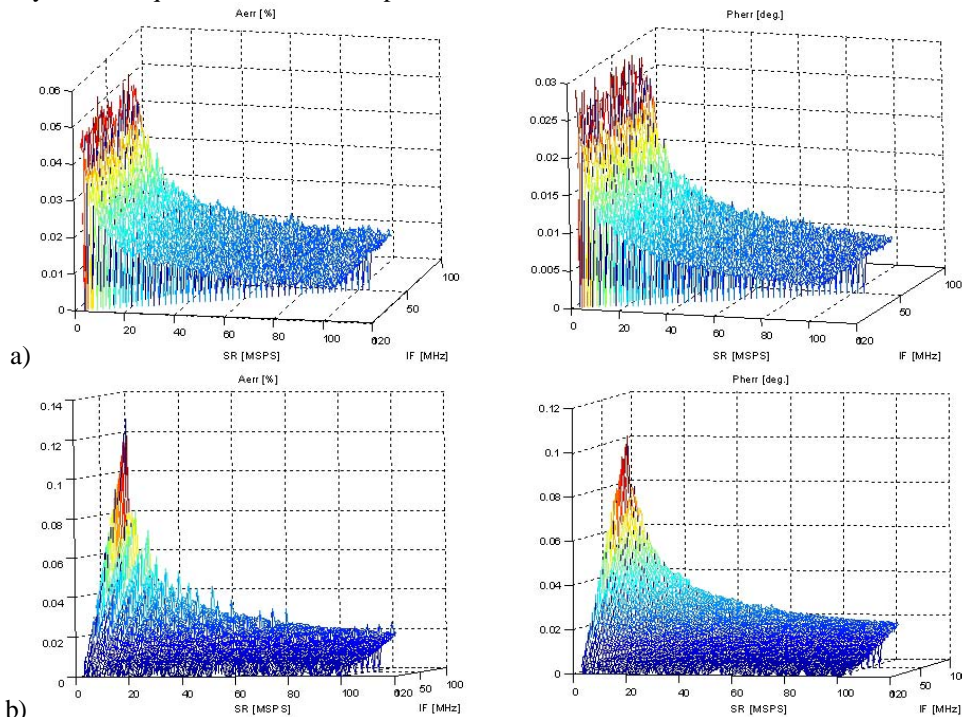


Fig. 2. Dependency of amplitude and phase errors on SR and IF (simulation results for averaging time 1µs) a) for 5ps clock jitter and b) for 5mV white noise

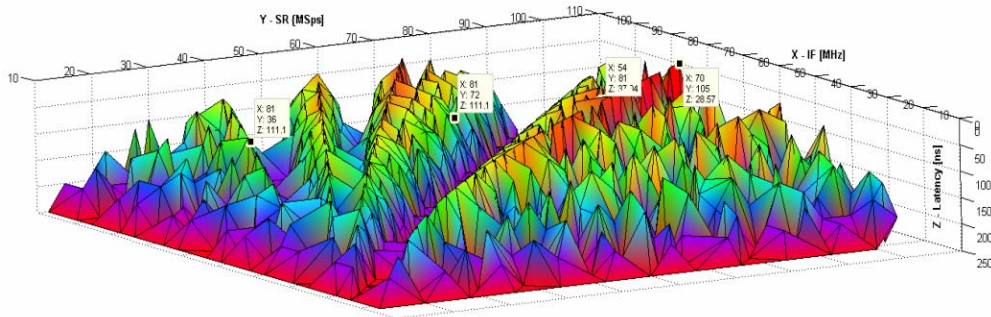


Fig. 3. Latency of IQ detection process in function of SR and IF (the drawing is simplified, only combinations of IF and SR that give latency less then 250 ns are presented)

CLOCK GENERATION

It is usually convenient to generate LO, IF and SR which are harmonically related, but with synthesizers is also possible to generate stable LO and clock signals which are related as (3):

$$f_1 = f_0 \times \left(\frac{n}{m}\right) \quad (3)$$

where n and m are integers. The frequency f_0 is the operating frequency but also subharmonics can be used as reference. If a laser master oscillator is used as phase reference, it will provide a pulse train at a repetition rate of 40-80 MHz. The operating frequency will be one of the higher harmonics and the next harmonic could be the LO because of its stability and simplicity of generation. An example for TESLA cavities operated at 1300 MHz is:

- $f_0 = 1300$ MHz (cavity operating frequency)
- $f_{mlo} = 50$ MHz (laser master oscillator rep. rate)
- $f_{if} = 50$ MHz (IF - intermediate frequency)
- $f_{lo} = 1350$ MHz (local oscillator frequency)
- $f_{clk} = 50 \times 3/2$ MHz = 75 MHz (SR - ADC clock)

The clock would allow measuring 3 samples in 2 IF periods and result in a measurement latency of 40ns plus the ADC conversion time of typically 3 clock cycles (40ns at 75 MHz).

CLOCK JITTER

The ADC clock signal is generated with a commercial LVDS converter and a Marconi signal generator. Measurements yield an estimation of timing jitter of ~2ps for SR=105MSPS and signal level -1dB under fullscale (dBFS) (Fig. 4).

CONCLUSION

The optimal choice of IF has to take into account several mutual influences between accuracy, latency, noise and jitter vulnerability. Since the IQ estimation error dependency on IF is dominated by ADC clock jitter over some IF limit it is convenient to set IF below or around this limit. On the other hand some combinations of IF and SR gives low latency in IQ estimation. For current system used in FLASH accelerator the the optimal IF is in the range of 50-70 MHz while sampling rate is set

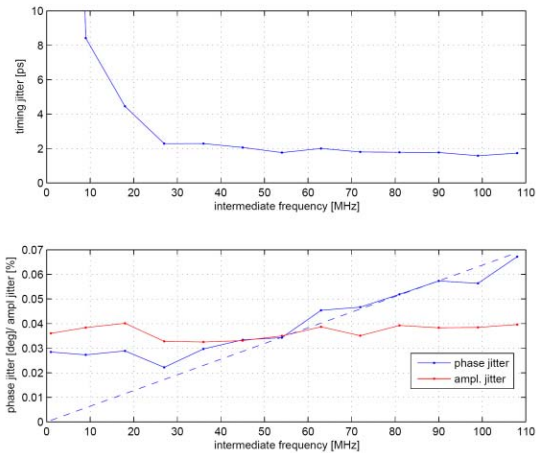


Fig. 4. Jitter dependency on IF

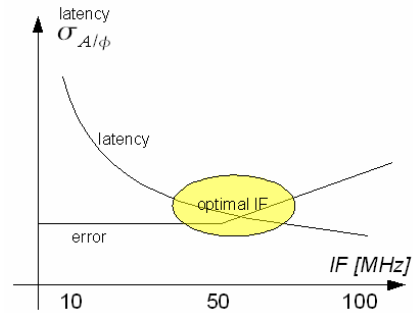


Fig. 5 The optimal frequency range for FLASH

in relation 3/2 of IF (that gives SR in the range 75-105 MSPs) (Fig. 5).

REFERENCES

[1] AD6645 data sheet. Analog Devices, www.analog.com
 [2] Grecki M., Jezynski T., Brandt A.: "Estimation of IQ Vector Components of RF Field - Theory and Implementation", Proc. 12th Mixed Design of Integrated Circuits and Systems, MIXDES 2005, Cracow, Poland. pp. 783-788