DEVELOPMENTS AT ELETTRA OF THE ELECTRONICS FOR THE BUNCH-ARRIVAL MONITOR

L. Pavlovic*, T. Korosec, M. Vidmar, University of Ljubljana, Ljubljana, Slovenia
M. Ferianis, F. Rossi, Sincrotrone Trieste, Trieste, Italy
K. Hacker, F. Loehl, H. Schlarb, DESY, Hamburg, Germany

Abstract

Within the framework of the EUROFEL project, a task has been started in 2006 for a joint development of a Bunch Arrival Monitor (BAM), based on the original idea from DESY. ELETTRA is responsible for the development of the VME-controlled clock-delay board of the BAM system. A variable clock-delay circuit (a phase shifter) is required to adjust the acquisition sampling point of the pick-up-modulated optical pulses of the master-laser oscillator. Since the optical pulses have a repetition rate of 40.625MHz (54MHz in the future) and the acquisition sampling frequency is double than this value, the clock-delay module operates in the 80-120MHz frequency range. The clock timing jitter of the acquisition system greatly affects the measurements: the output timing jitter from the clock-delay board should be less than 0.5ps-rms. Therefore, due to the very strict additive timing-jitter requirements, three phase shifter versions were designed, built and phase-noise evaluated. The low-pass-filter implementation achieved 563fs of total-system timing jitter (with source at 283fs), the integrated IQ multiplier 365fs (source jitter is 188fs) and the passive IQ modulator 265fs (source at 208fs).

INTRODUCTION

Bunch-arrival monitor (BAM) system designed at DESY, Hamburg, Germany, is based on the acquisiton of master-laser oscillator's (MLO) optical pulses, modulated by the electron-beam pick-up signal. Therefore amplitude changes of the acquisited signal corresponds to the beam (bunch) arrival time. Modulated laser pulses, converted to electrical signals using high-speed photodiodes, are sampled (acquisited) by a fast analog-to-digital converter (ADC), which requires suitable and phase-adjustable clock for adjusting the optimal sampling point. For this purpose clock-delay module was proposed in collaboration between DESY (Hamburg) and ELETTRA (Trieste) within EUROFEL DS3 design study. Block diagram of the test bench used at DESY for the bunch-arrival monitor is shown in figure 1.

Clock-delay module (CDM) is basically an electrically-adjustable phase shifter, with VersaModule Eurocard-bus (VME-bus) digital control and/or external analog control of the phase shifting. Input levels to the clock-delay module are from -30 to -10dBm. Since clock-delay module is used as a phase shifter for precise acquisition system, very strict output timing-jitter is required. For the DESY BAM test bench, the total output timing jitter from the CDM is defined as 500fs-rms.

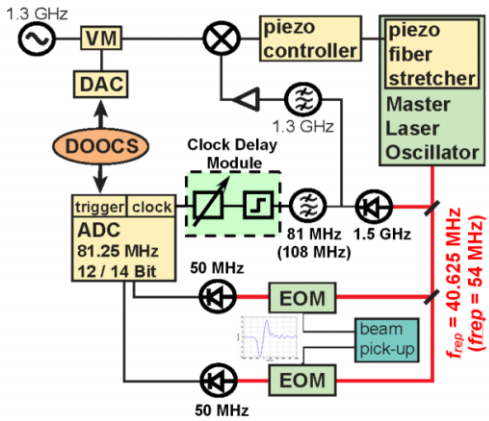

Figure 1: Block diagram of the bunch-arrival monitor test bench [1].

CLOCK-DELAY MODULE

The clock-delay module proposed is a VME-controlled phase shifter operating in the 80-120MHz frequency range. Beside digital control by VME bus, analog control is also possible by external inputs connected directly to the phase shifter using jumpers. The time step of the phase shifter is defined by digital-to-analog converter (DAC) resolution of 16-bits, which is sufficient to achieve the value of 500fs at 100MHz. For read-back and verification of the preset phase value, an analog-to-digital converter (ADC) is connected to the phase shifter control lines, again with 16-bit resolution. Output from the CDM is taken in a digital form with low-voltage positive emitter-coupled logic (LVPECL) and low-voltage differential signaling (LVDS) logic standard. Since both logic standards require DC coupling and 100Ω termination, proper connectors, interconnect cables and receiver front-ends must be used. An auxiliary output with 20dB gain from the input and sinewave waveform is added for test purposes. Block diagram of the clock-delay module is shown in figure 2.

* leon.pavlovic@fe.uni-lj.si

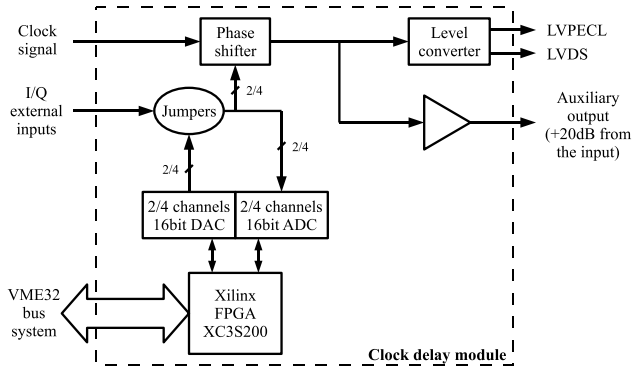

Figure 2: Block diagram of the clock-delay module.

CLOCK-DELAY MODULE PHASE-SHIFTER IMPLEMENTATIONS

Due to the fact that the BAM test bench requires stable and low-noise clock signal for precise acquisition system, three different phase-shifter variants have been designed, implemented and phase-noise evaluated.

Tunable low-pass filter as a phase shifter

First solution for the phase shifter is based on high-order tunable low-pass filter (LPF) with high cut-off frequency. Such filter has a variable amplitude and phase response resulting in phase shifting at the certain frequency. We have designed a 65^{th} order filter with high cut-off frequency assuring quite stable amplitude response (less than 3.5dB difference between the lowest and highest cut-off) and more than 360° phase shift in the range 80-120MHz. The designed filter is LC type built from fixed inductors and variable capacitors BB833. Varactors are biased with bias voltage from 0 to 9V to bring the desired performances.

The complete phase shifter design consists of a tunable low-pass filter itself, an input amplification stage and an output limiter as schematically shown in figure 3. For the final CDM implementation, a level converter at the output is also required, but it was omitted in this development stage.

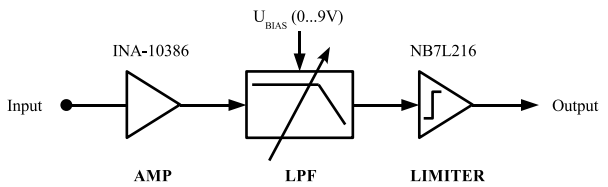

Figure 3: Block diagram of the low-pass filter as a phase shifter.

As the characteristic feature, phase noise and timing jitter of the overall phase shifter was measured at the input frequency of 100MHz. For comparison, the phase noise of signal oscillator and phase shifter output were measured. The obtained timing-jitter results are shown in table 1.

Table 1: Timing-jitter results of the low-pass filter as a phase shifter.

	Total timing jitter (10Hz-10MHz)
Anritsu MG3692B output	283 fs
Low-pass filter output	563 fs

Integrated IQ multiplier as a phase shifter

Using commercially available IQ multiplier ADL5390 from Analog Devices, IQ modulation is possible using an additional 90° splitter. Figure 4 shows a block diagram of the implementation of the phase shifter, operating in the frequency range from 80MHz to 120MHz, limited by the bandwidth of the power splitter. The DAC drives the IQ multiplier directly by differential I and Q signals for the best performance. The LVPECL and LVDS outputs are transformed to single-ended signals and AC-coupled for the direct connection to the phase-noise measurement equipment for the phase-noise evaluation.

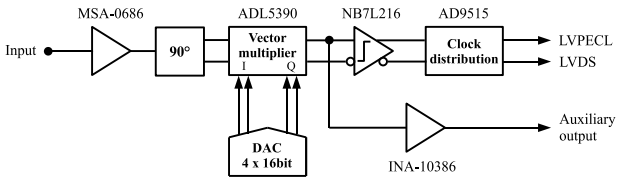

Figure 4: Block diagram of the integrated IQ multiplier as a phase shifter.

Total system timing-jitter results, computed from the phase-noise measurements, for the source and phase shifter output at 100MHz and -10dBm input power are shown in table 2.

Table 2: Timing-jitter results of the integrated IQ multiplier as a phase shifter.

	Total timing jitter (10Hz-10MHz)
Anritsu MG3692B output	188 fs
Integrated IQ multiplier output	365 fs

Passive IQ modulator as a phase shifter

Commercially available IQ modulator MIQC from Mini Circuits is used. Figure 5 shows a block diagram of the phase-shifter implementation, operating in the frequency range from 52MHz to 88MHz for the MIQC-88M part-number, limited by the bandwidth of the MIQC device. The DAC drives the IQ modulator using a low-noise operational amplifier. The LVPECL and LVDS outputs are transformed to single-ended signals and AC-coupled for the direct con-

nection to the phase-noise measurement equipment for the phase-noise evaluation.

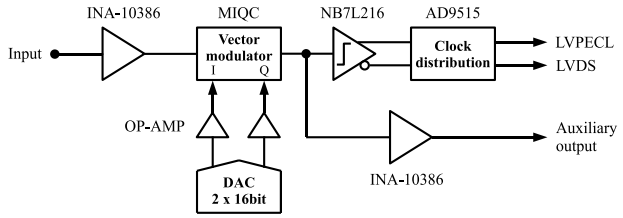

Figure 5: Block diagram of the passive IQ modulator as a phase shifter.

Total system timing-jitter results, computed from the phase-noise measurements, for the source and phase shifter output at 82MHz and -10dBm input power are shown in table 3.

Table 3: Timing-jitter results of the passive IQ modulator as a phase shifter.

	Total timing jitter (10Hz-10MHz)
Anritsu MG3692B output	208 fs
Passive IQ modulator output	265 fs

CLOCK-DELAY MODULE AS A STANDALONE VME-BUS CARD

The DESY control system used for the bunch-arrival-monitor set-up is based on a VME32 bus system. The module we are developing is a mixed signal board with an interface to this kind of bus system.

The analogue part of the board contains the circuits used to obtain the required phase shift values while the digital part has the interface to the bus system. The phase shifter can be driven by the VME bus or by external signals (jumpers located on the board). In this way the selection of the signal source for the phase shifter is manual: we have preferred this solution instead of another one (for example analogue multiplexers controlled by the VME bus) to reduce noise impairments on the phase shifter input signals.

The core of the board, which connects the two sections just described, is based on a programmable logic device, the XC3S200 chip from the Xilinx Spartan 3 family of FPGAs. The FPGA is programmed implementing a state machine for the interface to the VME bus (using the VME terminology, it's a slave module with A16 and D16 capabilities) and for the control of the 16-bits ADC/DAC chips. The ADC is used for monitoring operations while the DAC is actively used to drive the phase shifter section. The two interfaces to the analogue world are controlled by independent serial controllers.

CONCLUSIONS

Three different schemes of phase shifters were designed and phase-noise evaluated. Timing-jitter performance was found best with the passive IQ modulator version, where total system timing jitter measured was 265fs (the criteria for the BAM test bench is 500fs). The comparison of the phase noise profiles for the source and the output of the passive IQ modulator solution (measured with the Agilent E5052A) is shown in figure 6.

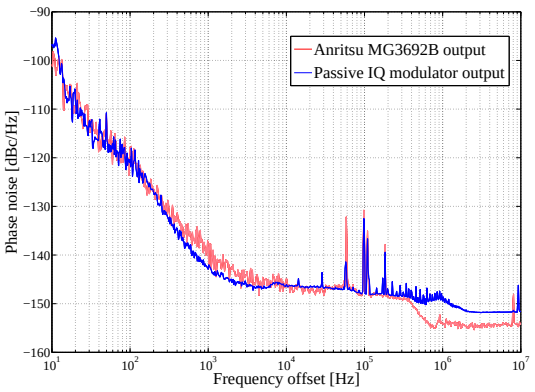

Figure 6: Phase noise profiles for the signal generator and the passive IQ modulator output.

However, additional phase-noise or timing-jitter improvement is possible with the optimization of the voltage levels between various stages in the analog section of the CDM (front-end amplifier, IQ modulator and level converter).

REFERENCES

[1] F. Loehl, K. Hacker, F. Ludwig, H. Schlarb, B. Schmidt, A. Winter, "A sub 100 fs electron bunch arrival-time monitor system for FLASH", Proceedings of EPAC 2006, Edinburgh, Scotland, 2006, pp. 2781–2783.