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Integrated Measurement Systems for Electronic Devices Operating in Radiation Environment

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Integrated Measurement Systems for Electronic Devices operating in Radiation Environment

Electronic systems in High Energy Physics experiments are exposed to radiation. Such hard environment provokes damages and errors in electronic devices. This M.Sc. thesis describes the radiation effects on different types of electronic components. Three measurement systems are presented, for irradiation experiments on Light Emitting Diodes, semiconductor memories (SDRAM and FLASH) and FPGA chips. Results of several tests that have been done are included and discussed.

Zintegrowane systemy do badań układów elektronicznych w środowisku o podwyższonym poziomie radiacji

Niniejsza praca obejmuje zagadnienia działania rożnych systemów elektronicznych pracujących w środowisku o podwyższonym poziomie radiacji, w eksperymentach Fizyki Wysokich Energii. Podjęte są najważniejsze kwestie związane z tą tematyką, gdyż problem całościowy jest zbyt obszerny i wykracza poza ramy tej pracy.

W części pierwszej (strona 13) przedstawiona została tematyka eksperymentów Fizyki Wysokich Energii. W doświadczeniach tych używane są skomplikowane układy elektroniczne do zbierania i przetwarzania danych oraz do kontroli i diagnostyki przeprowadzanych eksperymentów. Jak zostało pokazane środowisko w jakim urządzenia te muszą pracować jest szkodliwe dla wszelkich układów elektronicznych. Promieniowanie silnie wpływa na funkcjonowanie komponentów elektronicznych. Wynika stąd potrzeba zbadania tych zjawisk oraz próba tworzenia systemów o zwiększonej odporności radiacyjnej.

Kolejna część (strona 18) obejmuje opis efektów radiacyjnych w podzespołach elektronicznych. Szczegółowo zostały omówione trzy grupy tych efektów:

- Total Ionizing Dose (TID) (strona 18), powodowana przez neutrony, protony, ciężkie cząstki oraz promieniowanie gamma.
  Jest to efekt akumulacji promieniowania jonizującego. Prowadzi do zniszczenia komponentu elektronicznego.

- Single Event Effects (strona 19), powodowane pośrednio przez promieniowanie neutronowe.
  Prowadzi do nagłych błędów w układach lub całkowitego zniszczenia. Zjawisko wywoływania tego efektu przez neutrony zostało szczegółowo przedstawione w dodatkach (strona 66).

- Displacement Damage (strona 20), powodowane przez ciężkie lub wtórne cząstki.
  Jest to efekt strat niejonizującej energii (NIEL) wewnątrz układów przez oddziałujące cząstki. Powoduje zniszczenie struktury wewnętrznej komponentów.

W części trzeciej (strona 22) znajduje się szczegółowy opis zjawisk jakie zachodzą w komponentach elektronicznych będących obiektami badań przedstawionych w tej pracy. Są to:

- diody elektroluminescencyjne LED (strona 22),
- pamięci półprzewodnikowe (FLASH oraz SDRAM) (strona 23),
- układy programowalne FPGA (strona 26).

Promieniowanie protonów i neutronów (oraz innych cząstek powodujących NIEL) powoduje zniszczenie złącza p-n wewnątrz diody LED. Objawia się to zmniejszeniem jasności świecenia diody, po podłączeniu do stałego źródła prądowego. Dodatkowo wiadomo, że promieniowanie gamma nie powoduje zauważalnych zmian. Analizując budowę komórki pamięci FLASH (opartej na tranzystorze z pływającą bramką FAMOS) można sie spodziewać błędów związanych ze zniszczeniem struktury izolatora i odpłynięciem ładunku odpowiedzialnego za przechowywane dane. Prowadzi to do zmiany zawartości komórek pamięci FLASH. Możliwe są także uszkodzenia wewnętrznej logiki kontrolującej układ pamięci oraz pompy ładunków zapewniającej wysokie wartości napięcia potrzebne do zapisu lub skasowania zawartości pamięci FLASH. W pamięciach SDRAM elementem odpowiadającym za przetrzymywanie danych jest kondensator. W wyniku działania promeniowania radiacyjnego może zmieniać się potencjał tego kondenstora prowadząc do zmian w przechywanych danych. Także logika wewnętrzna, kontolująca układ, narażona jest na uszkodzenia. Układy FPGA są narażone na zniszczenia podobne do tych występujących w pamięciach SDRAM, ponieważ konfiguracja układu oparta jest na pamięci SRAM.

Z powyższych rozważań widać, iż układy elektroniczne pracujące w eksperymentach Fizyki Wysokich Energii, w środowisku radiacyjnym narażone są na szereg niekorzystnych zjawisk, uniemożliwiających ich pracę lub zmieniających ich funkcjonalność. Istnieje zatem potrzeba badań radiacyjnych takich urządzeń. Badania radiacyjne można podzielić na trzy etapy:

1. Pomiary poziomu radiacji.
2. Eksperymenty radiacyjne różnych układów i systemów elektronicznych.

3. Stworzenie systemu odpornego na zjawiska radiacyjne.

Niniejsza praca swoim zakresem zawiera się w punktach 1 i 2. Przedstawione są systemy pomiarowe i wyniki badań dla różnych podzespołów elektronicznych (układy FPGA, pamięci półprzewodnikowe, diody LED).

Cele tej pracy to:

- zrozumienie efektów radiacyjnych w układach elektronicznych,
- budowa cyfrowego fotomierza dla potrzeb dozymetru szybkich neutronów bazującego na diodach LED,
- budowa systemu pomiarowego dla statycznych błędów SEU w układach FPGA.

Część piąta (strona 32) niniejszej pracy przedstawia systemy pomiarowe dla wyżej wymienionych podzespołów elektronicznych. Dla diód elektroluminescencyjnych został skonstruowany system (strona 32) bazujący na mikrokontrolerze i składający się dodatkowo z fotomierza i źródła stałoprądowego. Pozwala on na pomiar wartości świetlności diody LED i w ten sposób wyznaczenie zniszczeń w jej strukturze wewnętrznej. Zostały także skonstruowane systemy do pomiarów wpływów radiacji na pamięci półprzewodnikowe (strona 38) oraz układy FPGA (strona 41).

Przeprowadzone zostały liczne badania radiacyjne wyżej wymienionych układów elektronicznych. Wyniki oraz procedury testowe przedstawione są w części szóstej (strona 44).

Uzyskane wyniki eksperymentów radiacyjnych pozwalają sformułować następujące wnioski:

- promieniowanie radiacyjne powoduje uszkodzenia w elementach elektronicznych,
- diody elektroluminescencyjne mogą być użyte jako detektory szybkich neutronów,
- największym problemem w układach pamięci SDRAM i układach FPGA są błędy SEU, powodowane przez neutrony,
- promieniowanie gamma jedynie zmniejsza trwałość ("czas życia") układów elektronicznych,

- w celu budowy systemów odpornych na zjawiska radiacyjne należy użyć odpowiednich technik zmniejszających wpływ promieniowania na układy elektroniczne.

Badania radiacyjne układów pamięci półprzewodnikowych FLASH i SDRAM pozwoliły na wybór odpowiedniej technologii dla potrzeb systemu trygera w eksperymencie CMS (CERN, Genewa).

W dodatkach zawarte są informacje, pozwalające zrozumieć dokładniej przedstawione w pracy zagadnienia:

- Opis miejsc i źródeł promieniowania użytych w badaniach, przedstawionych w niniejszej pracy. Są to:
  - cyklotron K130 na Uniwersytecie w Jyväskylä (Finlandia) (strona 61),
  - tunel akceleratora Linac II w DESY (Hamburg, Niemcy) (strona 62),
  - tunel akceleratora Tesla Test Facility II w DESY (Hamburg, Niemcy) (strona 63),
  - źródło promieniowania gamma ^{60}Co w instytucie Hahn-Meitner-Institut (Berlin, Niemcy) (strona 63),
  - nadprzewodzący medyczny cyklotron neutronowy K100 w szpitalu uniwersyteckim im. Harper'a (Detroit, USA) (strona 64),
  - źródło promieniowania neutronów $^{241}Am/Be$ (strona 65).
- Opis źródeł efektów radiacyjnych Single Event Upsets (strona 66).
- Pobieżny opis technik przeciwdziałania efektom radiacyjnym w układach elektronicznych, takich jak:
  - konwencjonalne przesłony redukujące promieniowanie (strona 68),
  - komponenty przeznaczone do pracy w środowisku o podwyższonym poziomie radiacji (strona 68),
  - odpowiednie techniki projektowe (strona 70).
- Ogólna charakterystyka zasad bezpieczeństwa radiacyjnego (strona 71).

Praca została uzupełniona o trzy artykuły, opublikowane w specjalistycznych periodykach, współautorstwa autora niniejszej pracy, które powstawały równolegle do przeprowadzanych badań:

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- D. Rybka, A. Kalicki, K. Poźniak, R. Romaniuk, B. Mukherjee, S. Simrock, *Irradiation Investigations for TESLA and X-FEL experiments at DESY*, Proceedings of SPIE, Volume 5775 (strona 94)

- D. Rybka, A. Kalicki, K. Poźniak, R. Romaniuk, B. Mukherjee, S. Simrock, *Investigations of Irradiation Effects on Electronic Components to be used in VUV-FEL and X-Fel Facilities at DESY*, Proceedings of SPIE, Volume 5948 (w procesie publikacji) (strona 112)

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Contents

1 Introduction

This thesis concentrates on different electronic devices operating in various radiation fields during High Energy Physics experiments. Presented work undertakes only the most important points, because total problem is very wide and exceeds over this thesis.

1.1 Particle physics and High Energy Physics experiments

Particle physics is a branch of physics that studies the elementary constituents of matter and radiation, and the interactions between them. Modern particle physics research is focused on subatomic particles, which have less structure than atoms. These include atomic constituents such as electrons, protons, and neutrons (protons and neutrons are actually composite particles, made up of quarks), particles produced by radiative and scattering processes, such as photons, neutrinos, and muons, as well as a wide range of exotic particles. [11]

It is also called High Energy Physics (HEP), because many elementary particles do not occur under normal circumstances in nature, but can be created and detected during energetic collisions of other particles, as is done in particle accelerators. [11] There are two basic types of particle accelerators [12]:

- Circular (eg. LHC, introduced later in this thesis) - particles move in a circle until they reach sufficient energy.
- Linear (eg. XFEL, introduced later in this thesis) - particles are accelerated in a straight line, with a target of interest at one end.

1.2 Electronics in modern High Energy Physics experiments

Electronic systems for High Energy Physics experiments can be divided in three corelated together functional groups [17]:

- Frontend electronics.
- Data processing and aqusition systems.

- Global systems.

This thesis ephasises problems of frontend electronics in radiation environment. Frontend systems are situated directly on the detectors or accelerators. These two cases are presented on examples of:

- CMS detector - electronic devices for trigger system,
- XFEL accelerator - electronic devices for controlling accelerator.

1.2.1 LHC collider and CMS experiment

The Large Hadron Collider (LHC) is a circular particle accelerator (27 km diameter), which is being developed at the CERN (European Organization for Nuclear Research) research centre in Geneva.

LHC is a collider which will probe deeper into matter than ever before. Due to switch on in 2007, it will ultimately collide beams of protons at an energy of 14 TeV. The LHC is the next step in a voyage of discovery which began a century ago. Accelerator will be built in the same tunnel as CERN's Large Electron Positron collider (LEP). Proton beams will be prepared by CERN's existing accelerator chain before being injected into the LHC.[15]

Five experiments, with huge detectors, will study what happens when the LHC's beams collide:

- ATLAS,
- CMS,
- ALICE,
- LHCb,
- TOTEM.

The problem of effects of radiation on electronic components will be presented on the example of CMS detector.

Electronics exposed to radiation in CMS experiment

The Compact Muon Solenoid (CMS) will be universal detector for LHC. It will allow to probe many particles appearing during the collisions in the collider. CMS will consist of many detectors.

Due to large amount of data from detector, frontend electronics and optical communication systems must be placed on the CMS detector, in the radiation environment. Radiation level was simulated and is presented in Table 1. [25]

Particles	At the barell	At the endcap
charged hadrons $E = 10 - 100MeV$	$3.6 * 10^1 cm^{-2}s^{-1}$	$1.6cm^{-2}s^{-1}$
neutrons $E > 20MeV$	$1.1 * 10^3 cm^{-2}s^{-1}$	$84cm^{-2}s^{-1}$
neutrons $E = 2 - 10MeV$	$7.2 * 10^2 cm^{-2}s^{-1}$	$93cm^{-2}s^{-1}$
neutrons $E > 100keV$	$4.4 * 10^3 cm^{-2}s^{-1}$	$370cm^{-2}s^{-1}$
neutrons $E < 100keV$	$1.1 * 10^4 cm^{-2}s^{-1}$	$650cm^{-2}s^{-1}$
neutrons total $E = 10 - 100MeV$	$1.7 * 10^4 cm^{-2}s^{-1}$	$1100cm^{-2}s^{-1}$

Table 1: Particle fluxes in regions of CMS detector where optical communication systems will be placed

1.2.2 X-FEL experiment

The X-ray free-electron laser (X-FEL) is linear accelerator, which is being developed at the DESY (Deutsches Elektronen-Synchrotron) research center in Hamburg, in cooperation with European partners. The facility could take up operation in 2012.

This facility will produce high-intensity ultra-short X-ray flashes with the properties of laser light. This new light source will open up a whole range of new perspectives for the natural sciences. The X-ray laser opens up unsuspected perspectives for physics, chemistry, materials science and geophysical research, biological sciences and medicine. The radiation is also of considerable interest to industrial users. [13]

Examples for research with the X-ray laser [14]:

- femtochemistry: capturing chemical reactions on film,
- structural biology: shedding light on biomolecules,
- materials research: developing new materials,
- plasma physics: a different state of matter,
- cluster physics,
- and many more.

Electronics exposed to radiation in XFEL tunnel

Some of electronic components (eg. low level radio frequency controllers) will be placed in the same tunnel as accelerator tube, as it is now in Tesla Test Facility II. Crates for these devices are situated in the catwalk (see Figure 1).

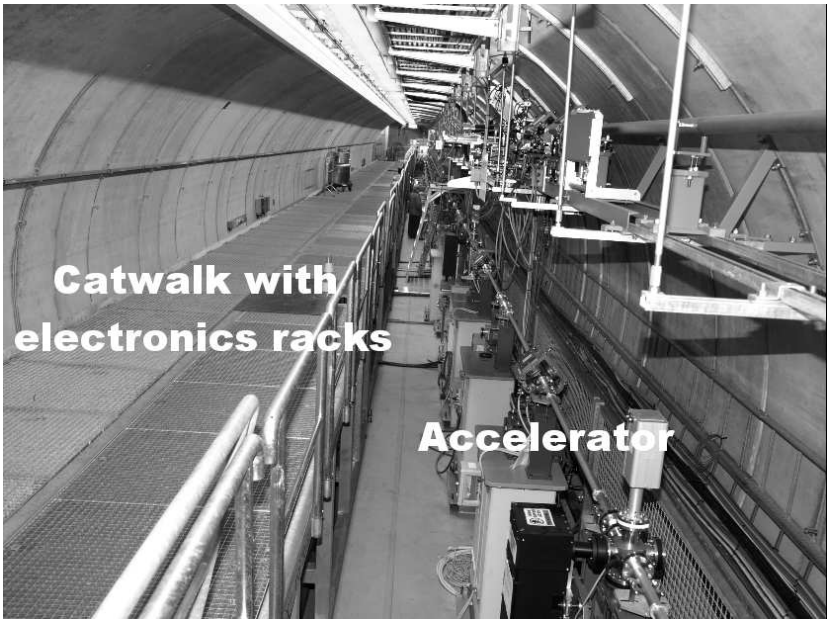

Figure 1: Tunnel of TESLA Test Facility II with crates for electronic systems in the catwalk

These devices will be exposed to parasistic pulsed radiation field, mainly due to [22]:

- beam loses in the tube,
- dark current from the superconducting cavities.

The roughly estimation of doses close to accelerating cryo module are to be [22]:

- 10^{12} neutrons$/$cm$^{-2}/20$ years
- 10 rad$/$hour for gammas (based on a maximum permitted additional cryo heatload of $0.1W/m^2$

2 Radiation effects on electronic components

Radiation causes damages in electronic components. The type and magnitude of these damages depend on irradiation environment. There are three main groups of mechanisms, the radiation effects in semiconductor materials [20][19][21]:

- Total Ionizing Dose (TID) effects,
- Single Event Effects (SEE),
- Displacement damage due to NIEL - Non Ionizing Energy Loss.

Briefly characteristics of these effects are presented in Table 2.

Effect	Caused by	Results	Time scale
TID	neutrons, protons, heavy particles or gammas	degradation of device as a function of ionizing radiation cumulation	long
SEE	high LET particles recoiled by neutrons	device upset or destruction	instantenous
NIEL	heavy or secondary particles	permanent damage of the semiconductor structure	medium/long

Table 2: Overview of the radiation effects in semiconductor devices

2.1 Total Ionizing Dose (TID) effects

Total Ionizing Dose effects are caused by neutrons, protons, heavy particles or gammas. It's degradation of device as a function of ionizing radiation cumulation.

Ionizing radiation causes electron-hole pairs creation in the oxides (see Figure 2). Some of these pairs recombinate, more in the absence of electric field. All remaining electrons, because of their high mobility leave the oxide. Holes, because of their very low mobility are mostly trapped. There is positive charge trapped in the oxide, resulting in the gradual degradation of the device.[20][19]

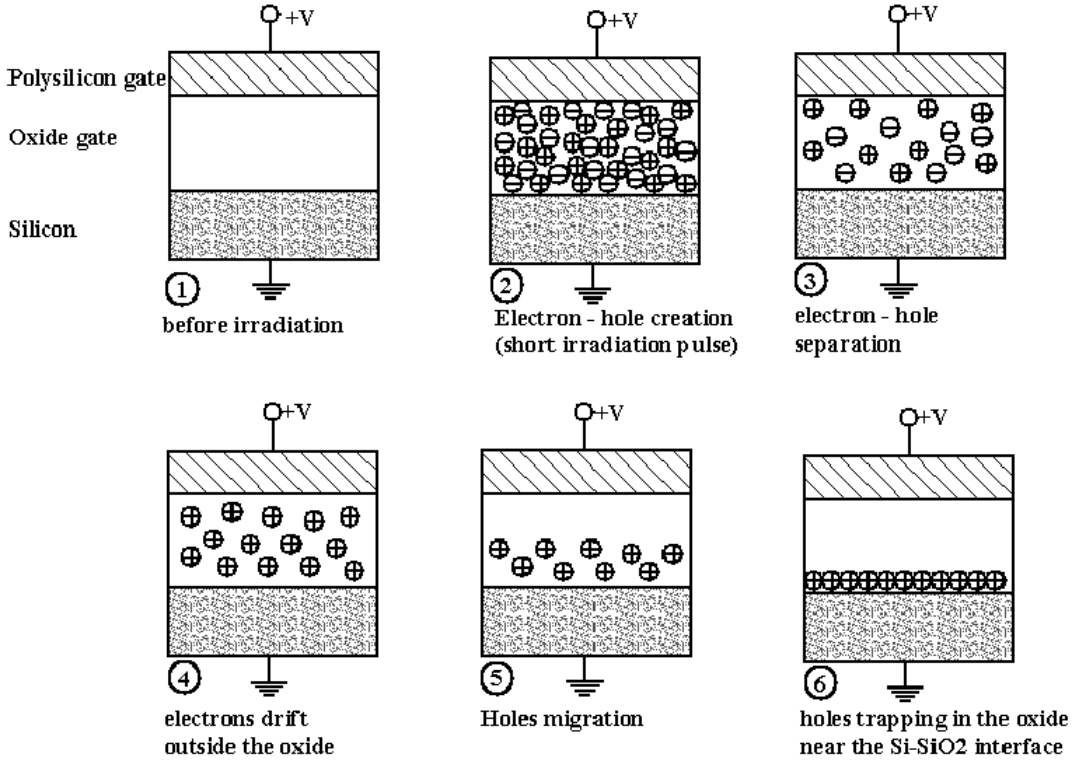

Figure 2: Cumulated ionization example in MOS oxide [20]

2.2 Single Event Effects (SEE)

Single Event Effects (SEE) can be generated by high LET (Linear Energy Transfer) particles recoiled by neutrons. It results in instantaneous device upset or destruction.

SEE occurs when highly ionizing particle penetrates through the oxide layer (see Figure 3). It provokes high electron-hole pairs density along its track and transient current across the oxide layer. In the results oxide breakdowns.[20][19]

There are different categories of Single Event Effects, depending on a place in the device where occur:

- with non-destructive results:
  - Single Event Upset (SEU) - bit flips in memory (see page 66),
  - Single Event Functional Interrupt (SEFI) - SEUs in device control logic (eg. in FPGA: JTAG TAP controller, Select Map interface),

  - Single Event Transient (SET) - changes in propagated signal,

- with destructive results:

  - Single Event Gate Rupture (SEGR) - gate-to-channel short circuit,
  - Single Event Burnout (SEB) - high instantaneous current → junction breakdowns,
  - Single Event Latch-up (SEL) - Vdd-to-Vss short circuit.

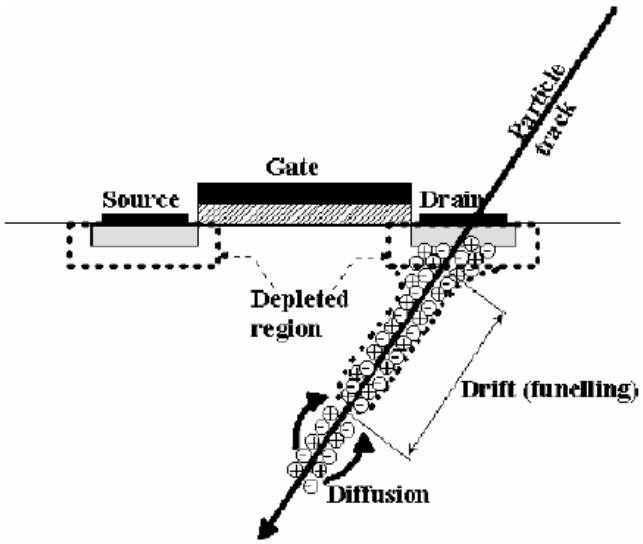

Figure 3: Example of Single Event Effect - Single Event Upset [20]

2.3 Displacement Damage due to NIEL - Non Ionizing Energy Loss

Displacement damages are caused by heavy or secondary particles. It's the result from particles producing Non Ionizing Energy Loss (NIEL).

Heavy or secondary particle collides with atoms from crystal structure of the semiconductor material. It causes defects in this structure along the track of particle.[20][19]

The effects of displacement damage could be:

- minority carrier's lifetime decreases,
- carrier's mobility decreases,

- effective majority carrier's concentration decreases - resistivity increases,
- creation of acceptor levels - type inversion (N → P).

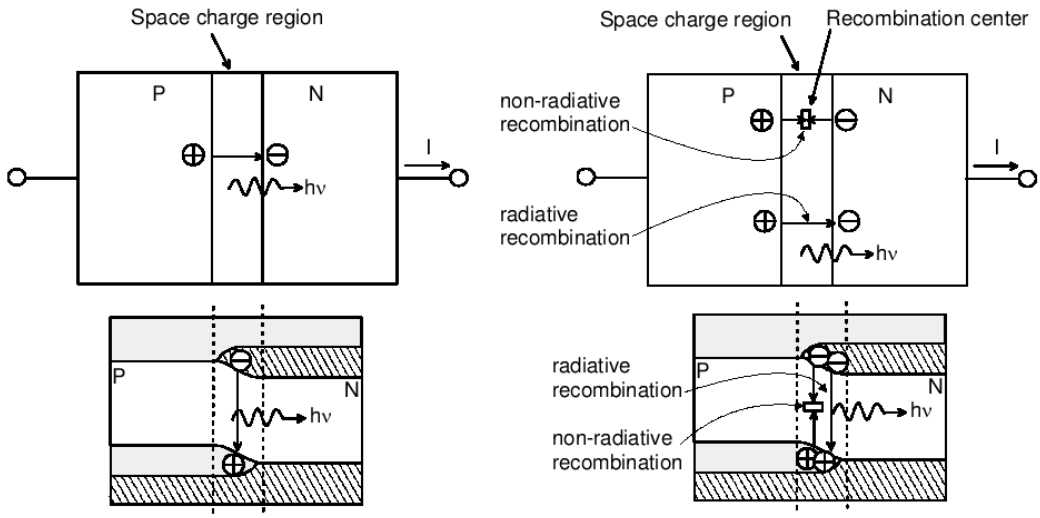

Figure 4: Creation of recombination center in P-N junction caused by displacement damage [20]

3 Radiation induced errors in electronic devices

This section describes radiation induced errors in electronic components. In details there are presented problems in devices, which are the objectives of radiation investigations presented in this thesis: Light Emitting Diodes, semiconductor memories (FLASH and SDRAM), FPGA chips.

3.1 Radiation induced damage in Light Emitting Diodes

Particles creating NIEL (Non Ionizing Energy Loss) causes the displacement damage in p-n junction of semiconductor devices, such as Light Emitting Diodes (LEDs). As the effect there is less luminescence of irradiated (e.g.: with protons, neutrons) LEDs, connected to constant current source. This permanent effect is much more noticeable than damages created after irradiation with gammas (see Figure 5, where KERMA - Kinetic Energy Released in Matter) [21][7][18].

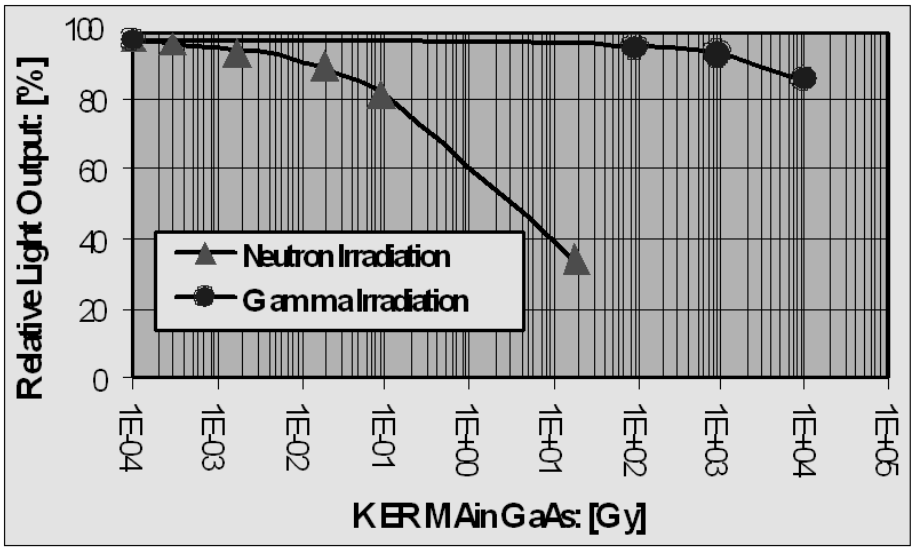

Figure 5: Relative light output of GaAs LED irradiated with ^{60}Co gamma rays ($E_g = 1.25MeV$) and fast neutrons ($E_n = 16MeV$) from a medical cyclotron[18]

3.2 Radiation induced errors in semiconductor memories

Depending on type of semiconductor memories there are different effects supposed to be induced in FLASH and SDRAM memories.

3.2.1 FLASH memories

In FLASH memories there are transistors with a modificated floating gate (FAMOS - Floating gate Avalanche-injection MOS) to store data (see Figure 6). Operation of the FAMOS transistor is based on the Fowler-Nordheim tunnelling of charge carriers from a source (drain) through the oxide to its floating gate.

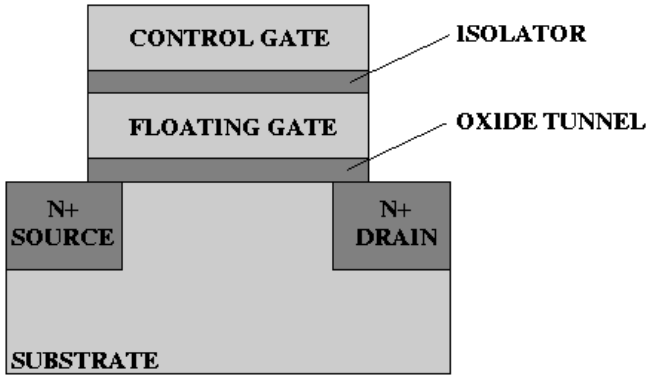

Figure 6: FAMOS transistor cross section

The writing operation injects electrons into the floating gate through the oxide layer. The erasing operation removes them from the floating gate. During erasing all bits are set to ’1’. The writing operation sets the bits to ’0’, thus the writing can be done only after erasing. [44]

Voltages required for writing and erasing operations (+12V, +7V and -9V) are higher than the power supply voltage. There are provided by the charge-pump circuit. A degradation of this subsystem of memory chip is very probable in a radiation environment, because the charge-pump works with relatively high voltages.

Ionizing radiation can destroy the isolator structure, allowing the charge accumulated in the floating gate to migrate out of it. As the result the memory cell changes its state from ’0’ to ’1’. There is no mechanism changing the state of a memory cell from ’1’ to ’0’. [31][36][37][30]

In the FLASH memory chip there are several registers and some logic, controling the memory, which are also vulnerable to radiation (see Figure 7).

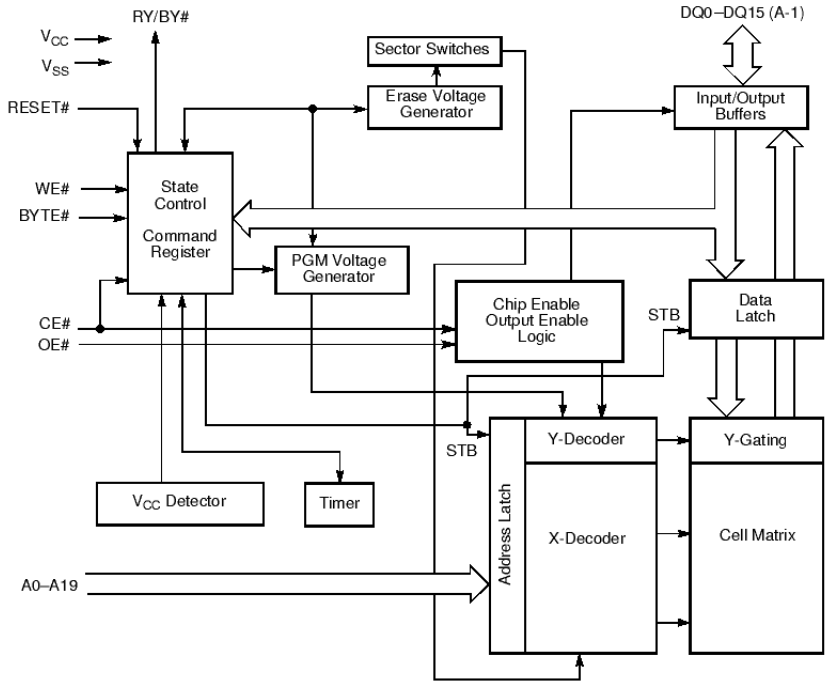

Figure 7: Schematic block diagram of Am29LV160D FLASH memory [45]

3.2.2 SDRAM memories

SDRAM (Synchronous Dynamic Random Access Memory) uses a capacitor as a data storage element and a transistor as a switch (see Figure 8). When the potential of the capacitor is at ground level, the state of the cell is ’0’. When this potential is equal to the supply voltage, the state of the cell is ’1’.

In a radiation environment, ionizing particles passing through the capacitor generate electron-hole pairs. The potential on the capacitor may then change, changing the memory state. This type of errors - SEUs - are the most frequent errors in SDRAMs [32][33]. Futhermore, two types of SEUs are observed:

- recoverable bit upsets - single or multiple errors in one word of memory,
- stuck bits - bits, which do not change their state even after reprogramming.

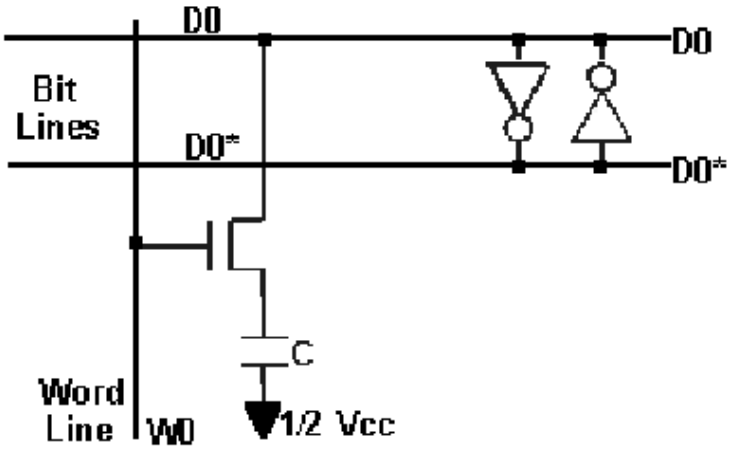

Figure 8: SDRAM memory cell

In the SDRAM memory chip there are several registers and some controlers of the memory, which are also vulnerable to radiation (see Figure 9).

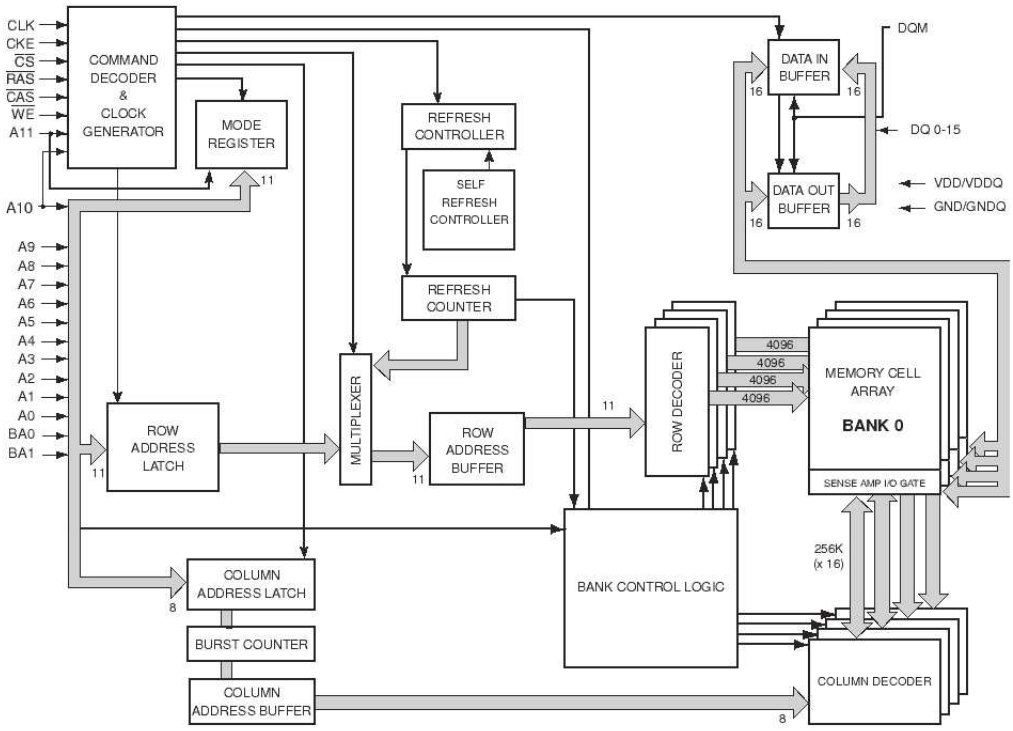

Figure 9: Block schematic of IS42S16400 SDRAM memory [46]

3.3 Radiation induced errors in FPGA chips

In this section the FPGA chips architecture is briefly presened. Single Event Effects in these devices are discussed.

3.3.1 FPGA architecture

Field Programmable Gate Array chips (FPGA) are type of programmable circuits, which are programmed by user to perform the designed functionallity. Project must be written in one of Hardware Description Language (HDL), e.g. VHDL, Verilog. It's compiled, synthesized and implemented in FPGA chip. The configuration bits can be stored in a chip using different techniques depending on technology [54]:

- Antifuse technology - programmable only once,
- Flash memory - programmable several times,
- SRAM memory - programmable dynamically.

The last possibility is dominating technology. It allows very fast, almost unlimited in system reprogramming.

Architecture of FPGA chips from different vendors may differ but the main idea is almost the same. It consists of some main blocks (description based on Xilinx Spartan-IIE chip, see Figure 10) [55]:

- Flexible, programmable Configurable Logic Blocks (CLB), which provide the functional elements for constructing logic. The basic block of the CLB is Logic Cell (LC). Two LCs form slice and two slices form CLB. Each LC includes a function generator, carry logic and a storage element. The function generator is implemented as look-up table (LUT). The storage element can be configured either as edge-triggered D-type flip-flop or as level-sensitive latch.
- Programmable Input/Output Blocks (IOB), which provide the interface between the package pins and the internal logic. The IOB features inputs and outputs that support

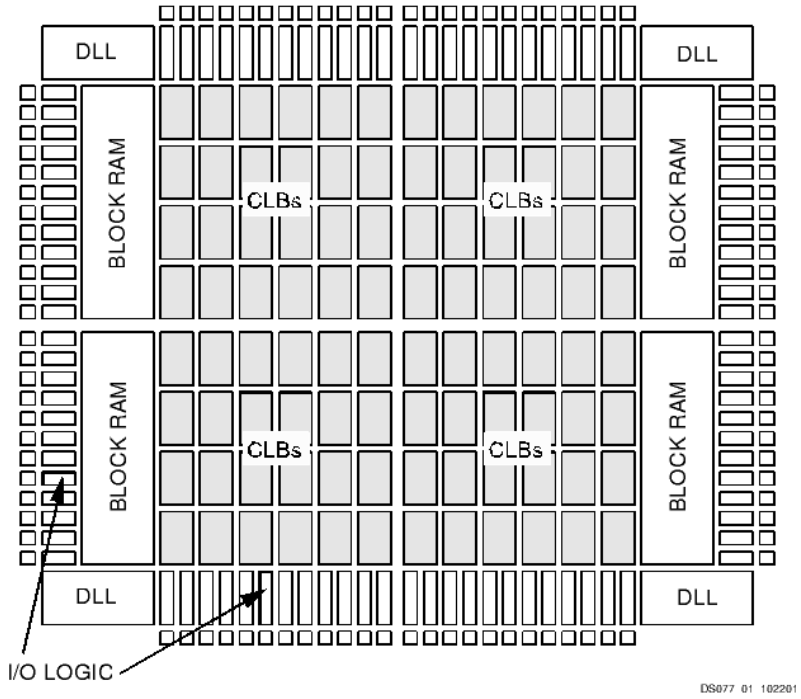

Figure 10: Basic Spartan-IIE Family FPGA Block Diagram [55]

a wide variety of I/O signalling standards. Each input and output can be configured to conform any of the low-voltage signalling standards.

- Delay-Locked Loops (DLL) for clock distribution. This blocks eliminate skew between the clock input pad and internal clock-input pins throughout the device. Additionaly delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input.

- Dedicated internal memory (Block RAM). This memory can be used to storage data inside the chip. The word length and type of memory is configured by system designer.

- Versatile multi-level interconnection structure. Local routing resources provide three types of connections:

  – interconnections among the LUTs, flip-flops,

  – internal CLB feedback paths, between LUTs in the same CLB,

– direct paths providing high-speed connections between horizontally adjecent CLBs.

The software automatically uses the best available routing based on user timing requirements.

Values stored in static memory cells control all the configurable logic elements and interconnection resources. These values must be loaded into the memory cells on power-up and can be reloaded to change function of the device, almost any time.

3.3.2 Single Event Effects (SEE) in FPGA chips

SRAM (Static Random Access Memory) cells in FPGA and internal flip-flops have similar structure to SDRAM memory cell (see Figure 8) and are immune to radiation. The most probable effects in FPGA chips are Single Event Effects, especially Single Event Upsets.

Single Event Upset (SEU) is a change of the logic state of an element storing one bit caused by radiation. Two types of SEUs may be distinguished (see Figure 11):

- static SEUs - changes in the configuration bits,
- dynamic (or transient) SEUs - changes in the logic state of the bits, which are supposed to change during normal operation (for example flip-flops).

SEUs affect the performance of FPGA in different ways. Changing the state of one flip-flop working as a latch results in a false value of one bit during one clock period only, while changing the state of one SRAM cell in the look-up table results in a permanent wrong answer for one combination of input bits. Changing the state of one SRAM that programs the interconnection between logic blocks can seriously modify the performance of whole circuit. [35][38]

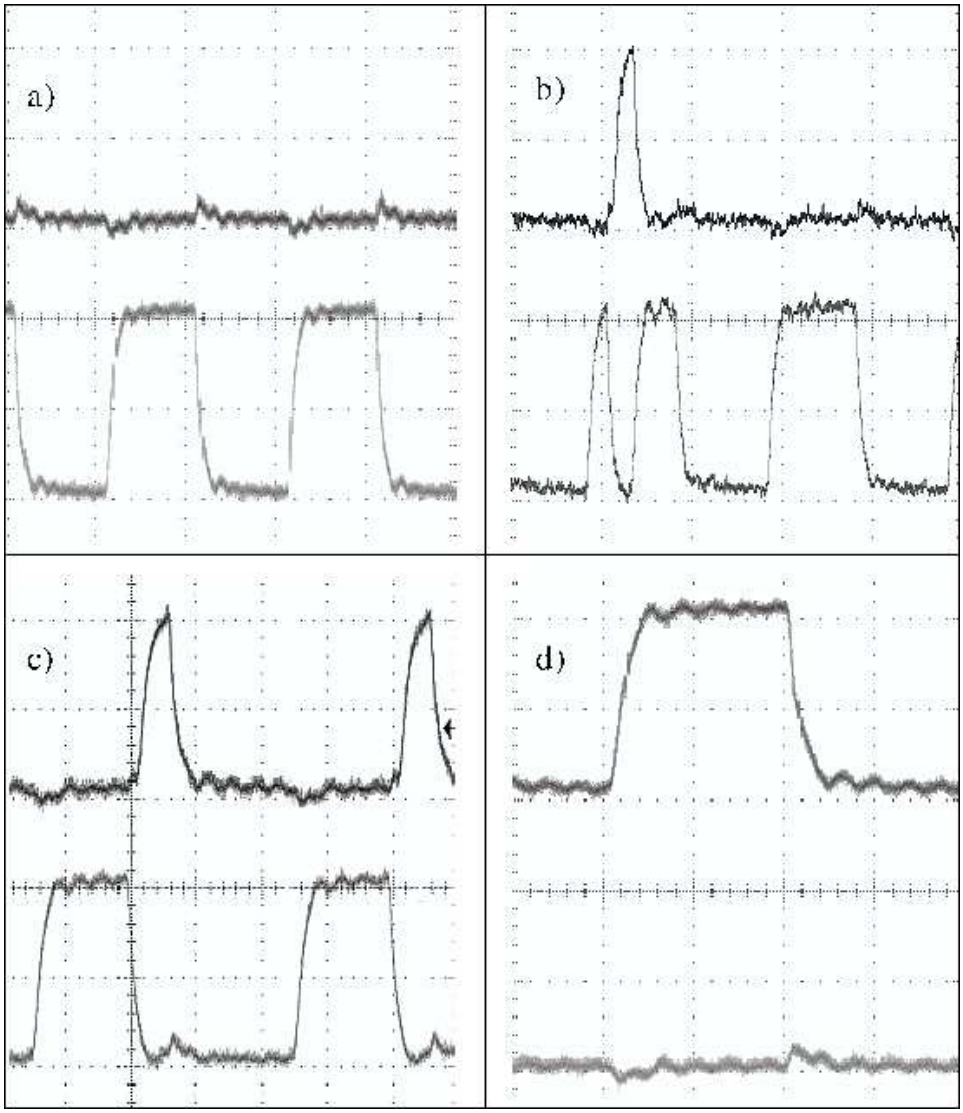

Figure 11: Examples of SEUs in the shift register design observed on the scope. Upper signal - the SEU indicator, bottom signal - the output of the shift register. a) normal operation; b) dynamic SEU ; c) static SEU - the shift register broken off and linked to other part of register; d) static SEU - the shift register broken off, input of register connected to ’0’.[1][2]

4 Thesis' objectives

A significant number of electronic systems for controling and diagnostics of modern HEP experiments (such as CMS, VUV-FEL, X-FEL, ILC) are ussually located in the accelerator tunnel, next to the accelerating tube, producing various radiation fields. In such environment problems with these systems are expected to occur. The studies on electronic components' radiation sensivity are needed. These investigations should provide vital information to optimize the design of electronic systems and to minimalize failures during long-term operation. [22]

The irradiation experiments could be divided into three steps [3][4][5]:

1. Radiation level measurements:
    - evaluation of radiation level,
    - understanding the radiation effects in accelerators (especially: superconducting linacs) and measurements of radiation level (neutrons, gammas).
2. Investigations of radiation effects on electronic components, circuits and complete systems:
    - determine Single Event Effects (SEEs),
    - determine Total Ionizing Dose (TID) effects,
    - determine radiation effects on different types of electronics,
    - predict performance and life-time of electronics in radiation environment.
3. Counter measures:
    - development of radiation mitigation concepts and evaluate their performance in the presence of radiation.

This thesis partially fulfills points 1 and 2 of presented scheme of work. There are described measurement systems for irradiation experiments of electronic devices, such as:

- FPGA (Field Programmable Gate Array) chips,
- semiconductor memories (SDRAM and FLASH),
- LEDs (Light Emitting Diodes).

Results of experiments are included and discussed.
The main objectives of thesis as follows:

- Understanding the radiation effects on electronic components.
- Development of digital photometer for the evaluation of COTS (Commercial-Off-The-Shelf) LED (Light Emitting Diodes) fast neutron dosimeter.
- Development of the test system for SEUs (Single Event Upsets) in FPGA (Field Programmable Gate Array) chips.

5 Measurement systems for electronic devices operating in radiation environment

We have developed three measurement systems for radiation experiments with electronic devices. First is a part of Commercial-Off-The-Shelf Light Emitting Diodes fast neutron dosimeter. It supports measuring light output from Light Emitting Diodes and calculating ratio of its degradation after irradiation with fast neutrons. Second test system was developed for experiments with semiconductor memories. Third measurement system allows us to investigate static Single Event Upsets in FPGA chips during irradiation.

5.1 Digital photometer for Commercial-Off-The-Shelf Light Emitting Diodes fast neutron dosimeter

The proposed experiment goal was to investigate the radiation damage phenomena of the Light Emitting Diodes irradiated with accelerator produced fast neutrons. Two measurements should be done:

- before irradiation,
- after irradiation.

The neutron flux could be further estimated using light attenuation (ratio between this two values) and calibration data.

We have built two devices:

- prototype test system, based on laboratory measurement instruments,
- specialized device based on microcontroller.

5.1.1 Prototype test system

The prototype instrument consisted of (see Figure 12):

- photometer (RS V10860, supplier: RS Components),

- power supply (EA-PS 2016-050, supplier: Conrad Electronic),
- digital multimeter (HP 34401A, supplier: Hewlett-Packard),
- custom designed aluminium cup.

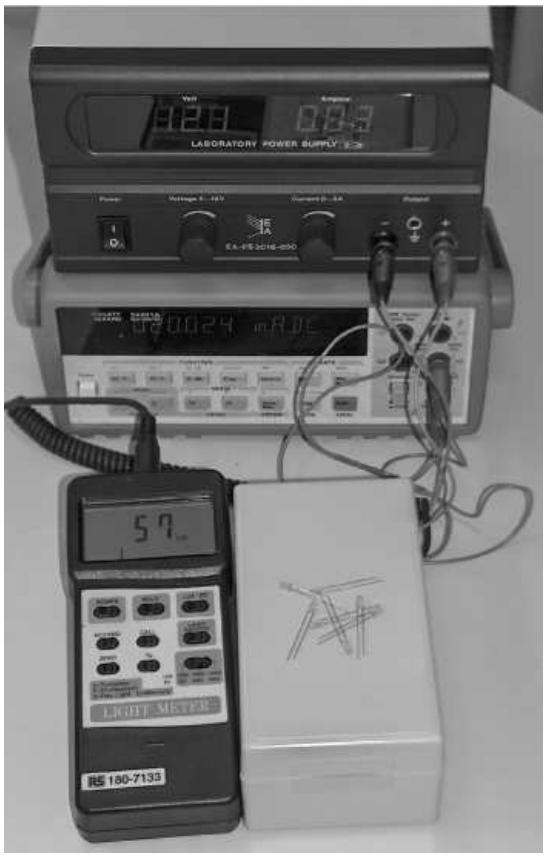

Figure 12: Prototype test system for COTS LED fast neutron dosimeter

The prototype measurement system was used for preliminary investigations, to prove that method of quantify neutron flux using degradation of light emission from Light Emitting Diodes works.

5.1.2 Device schematic

The device consists of three sections (see Figure 13):

- mictrocontroller,

- constant current supply,
- photometer.

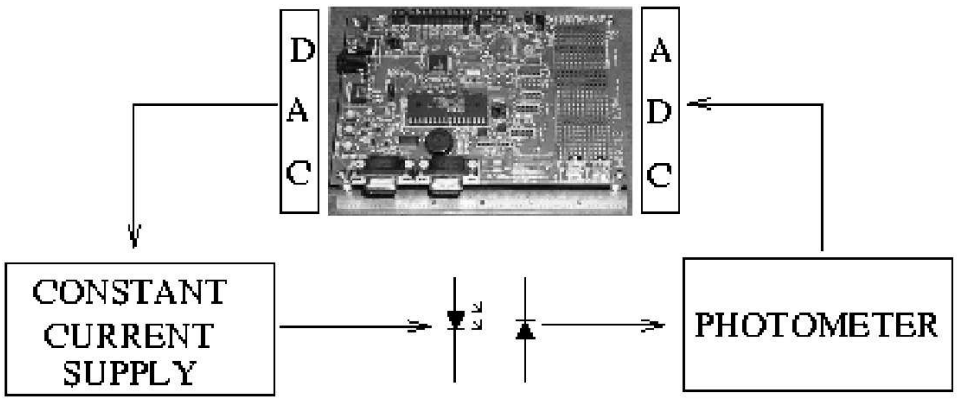

Figure 13: Block diagram of digital photometer for COTS LED fast neutron dosimeter

The device utilizes Texas Instruments MSC1211 Evaluation Module (see Figure 14) [47]. MSC1211 is precision analog to digital converter with 8051 microcontroller and FLASH memory inside [48].

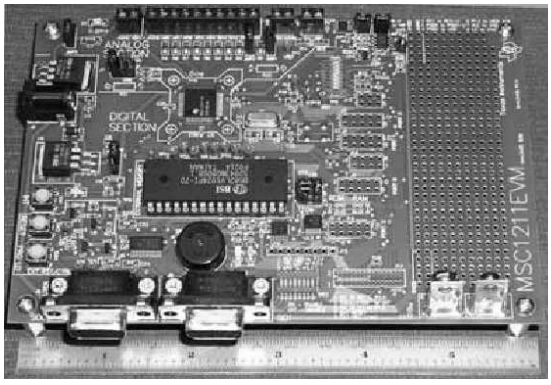

Figure 14: Texas Instruments MSC1211 Evaluation Module

Main features of module, which are used in project:

- 8051 microcontroller,
- 24-bit delta-sigma analog-to-digital converter,

- 16-bit digital-to-analog converter,
- serial port driver.

Microcontroller gives signals to the constant current supply to provide current for the measured LED and to the photometer to measure illuminance. It also communicates with PC computer through the serial port.

The constant current supply (see Figure 15) supplies current for measured LED. This current source gives 13 mA for every supplied diode.

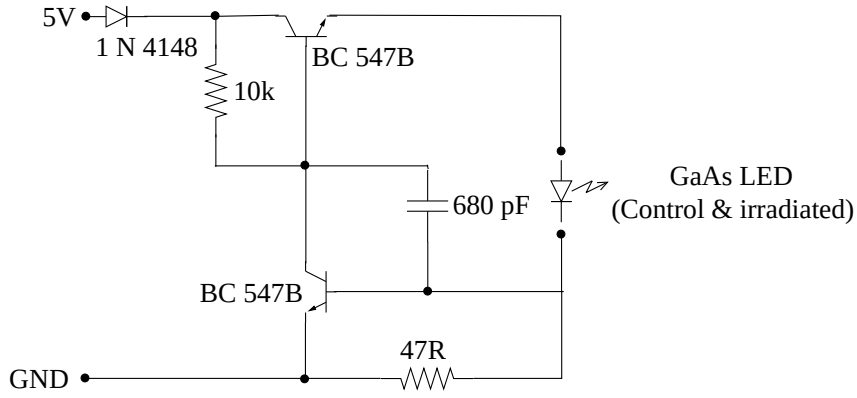

Figure 15: Schematic of constant current supply for digital photometer for COTS LED fast neutron dosimeter

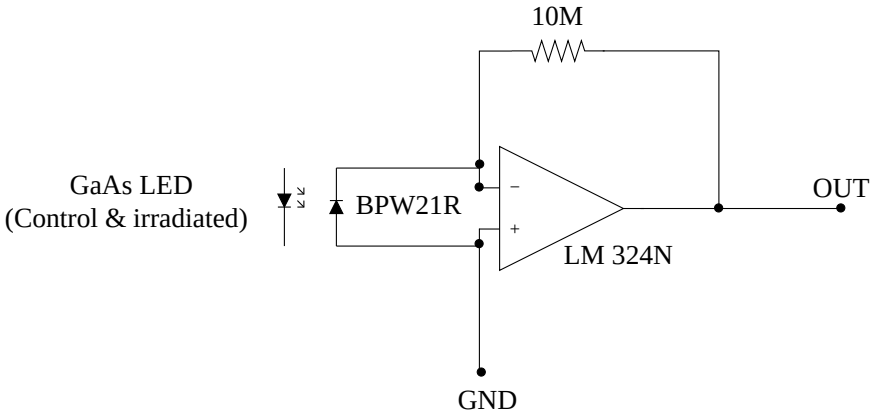

Figure 16: Schematic of photometer for digital photometer for COTS LED fast neutron dosimeter

The photometer section (see Figure 16) is based on planar Silicon PN photodiode BPW21R from Vishay Semiconductors [49]. This model was chosen because of its high sensivity and excellent linearity.

The precision operational amplifier was used to amplify measured value of illuminance. As this element there was used LM324 from STMicroelectronics [50].

Assembled digital photometer for COTS LED fast neutron dosimeter with special cup to hold LEDs is presented on Figure 17.

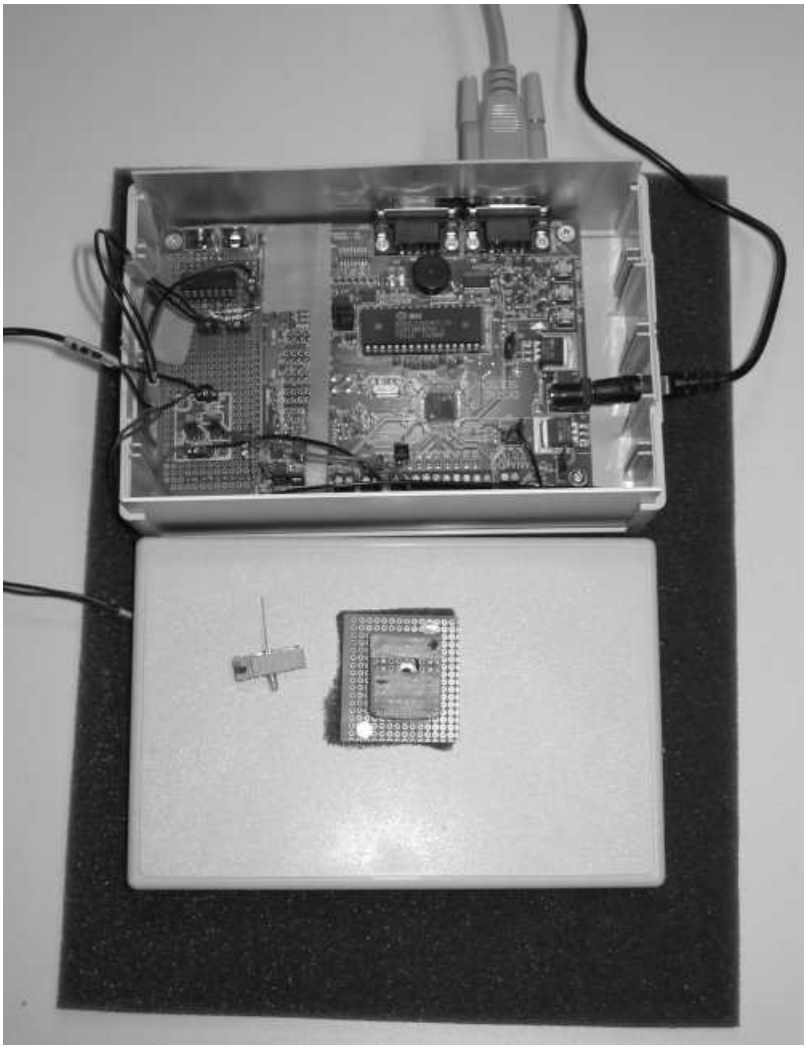

Figure 17: Assembled digital photometer for COTS LED fast neutron dosimeter with LED holder

5.1.3 Control application

The single measurement consists of:

- measurement trigger from PC,
- grabbing data from photodiode during flashes of measured LED,
- sending results to PC computer.

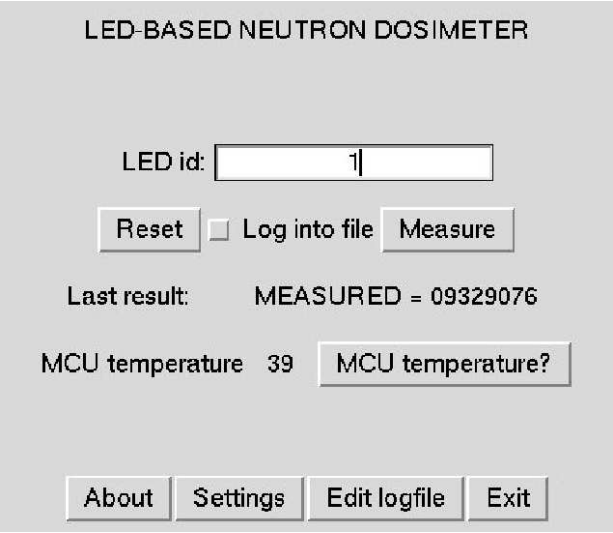

Figure 18: Control application panel for digital photometer for COTS LED fast neutron dosimeter

We have developed a dedicated software (see Figure 18) for controlling device using PC computer connected to instrument by serial port. The software was written in Python language using Tix/Tkinter libraries for Graphic User Interface (GUI).

Functions available in application:

- resetting the device,
- performing measurement,
- measuring microcontroler temperature,
- logging measurements to file with specific ID code for each LED.

5.2 Test system for investigations of Single Event Upsets in semiconductor memories

Measurement system for investigations of Single Event Upsets in semiconductor memories was developed in cooperation with Wojciech Zabołotny, Krzysztof Poźniak from Warsaw University of Technology and Maciej Kudła, Krzysztof Kierzkowski, Karol Buńkowski from Warsaw University. Software was written in cooperation with Wojciech Zabołotny.

5.2.1 System schematic

Test board (see Figure 19) consists of:

- FPGA chip (Altera ACEX 1K EP1K100FC256) [51],
- microcontroler (AVR AT90S8515) [52],
- SDRAM memory,
- ZIF socket for removable FLASH memories.

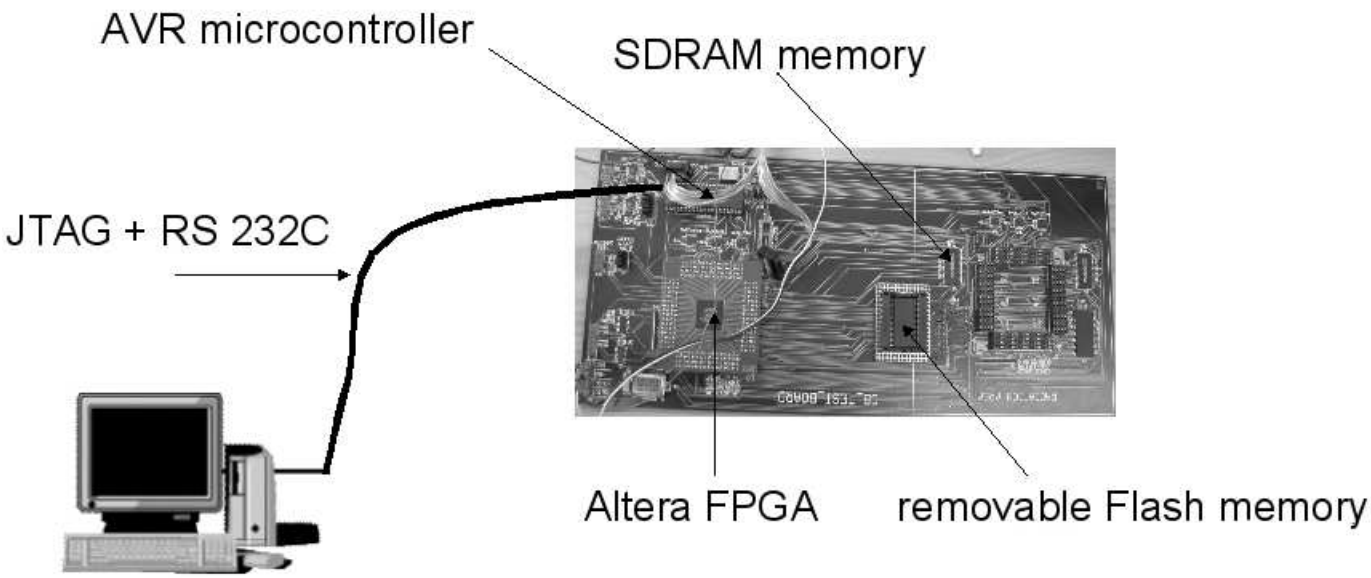

Figure 19: Test system for investigations of Single Event Upsets in semiconductor memories

5.2.2 Hardware

The AVR microcontroller was used to perform tests of the memories and to report errors to PC computer. FPGA chip worked as FLASH and SDRAM memories controller and random number generator. Devices communicated through internal bus.

FPGA had numerous registers:

- FPGA command, status registers,
- FLASH adrress, data, status registers,
- SDRAM adrress, data, status registers,
- random number generator register.

It allowed to perform some commmands, written to command register:

- reset FPGA,
- erase, write, read FLASH memory,
- write, read SDRAM memory,
- write, read, cycle random number generator.

Chip was programmed using JTAG port and Jam Player software.

Code for the microcontroller was written in C language and compiled with AVR-GCC software. The device was programmed using UISP interface. The microcontroler communicates with PC computer by the serial port (RS 232C). Following functions were implemented:

- read and write serial port,
- read and write FPGA registers,
- read, write, initialize and test FLASH memory,
- read, write, initialize and test SDRAM memory,
- initialize, read and cycle random number generator.

5.2.3 Control application

Dedicated application (see Figure 20) was written in Python language, using Tix/Tkinter libraries for building Graphic User Interface. It was used for communication with microcontroller and controlling the experiment. The software allows to:

- program and reset the microcontroller,
- program and reset the FPGA chip,
- set the random number generator,
- fill the memories with random values,
- start and stop test,
- communicate with microcontroller using serial port and low-level commands.

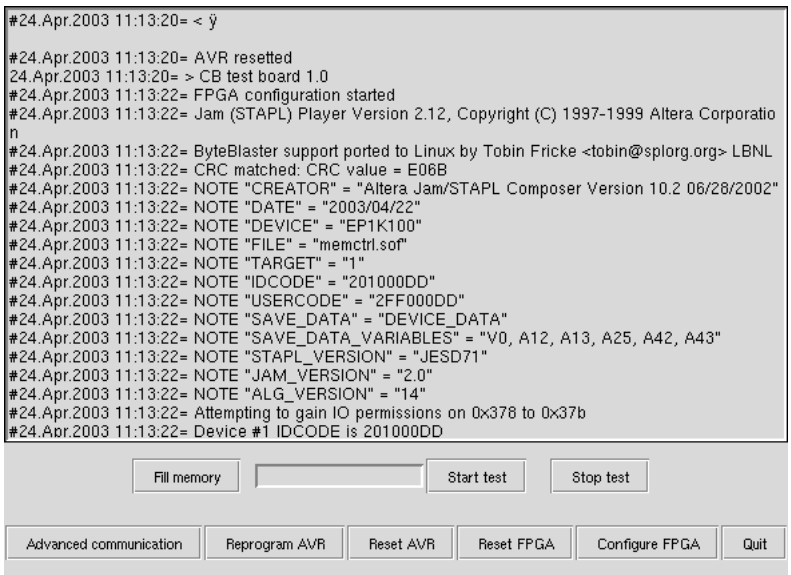

Figure 20: Application for investigations of Single Event Upsets in semiconductor memories

All commands and output data from microcontroller were logged into file and displayed in the application window.

5.3 Test system for investigations of static Single Event Upsets in FPGA chips

Because of higher incidence of static Single Event Upsets in FPGA chips than the dynamic one, test system was built for static SEUs [1][2]. Many attemps of dynamic SEUs investigations had failed. Main reason is the high complexity of the device. FPGA chips have a lot of internal connections, registers and configuration memory, all are based on SRAM technology. Because of higher probability to observe errors in these elements dynamic SEUs are hard to notice.

5.3.1 System schematic

Test system for investigations of static Single Event Upsets in FPGA chips consists of (see Figure 21):

- PC computer running dedicated software,
- JTAG → RS 485 signals converter board,
- RS 485 → JTAG signals converter board,
- Device Under Tests (DUT).

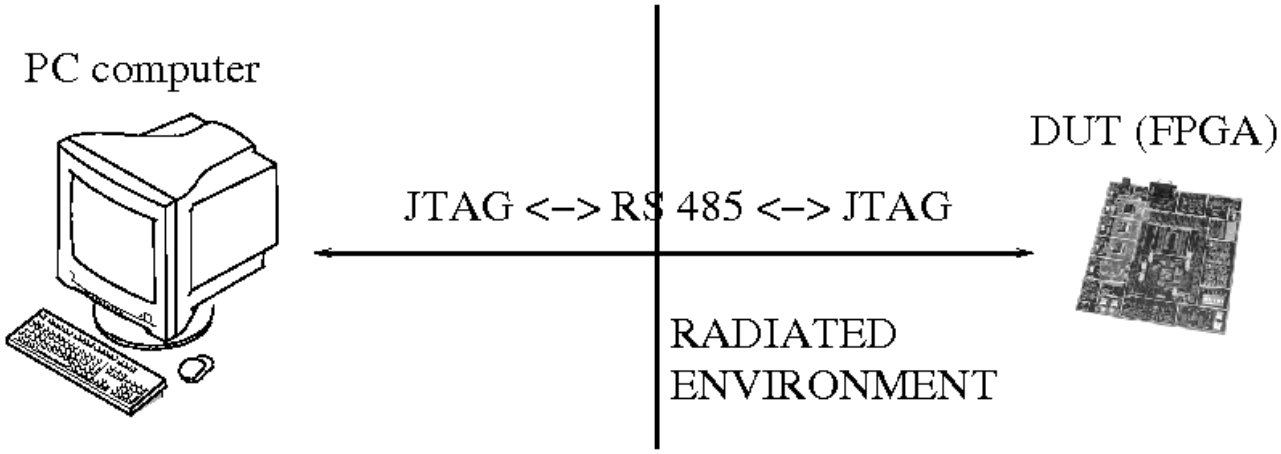

Figure 21: Test system for investigations of Single Event Upsets in FPGA chips

5.3.2 JTAG ↔ RS 485 converters

The PC with software to control irradiation experiments on the FGPA chips was placed outside the radiation area, far away from DUT. The JTAG signals doesn't allow to be tranfered using long cables. Two converter boards were developed to use RS 485 signals instead of JTAG. It allowed to extend range of cables and to put PC computer in safe place.

5.3.3 Investigation method of static Single Event Upsets in FPGA chips

Static Single Event Upsets in FPGA chips can be investigated using readback function. This functionality allows to get from device the configuration memory. At the begining FPGA is programmed with dummy logic. Then the reading of configuration is done continuously. The bitstreams (programmed and read) are compared. The number of different bits indicate the number of static Single Event Upsets in configuration memory of device.

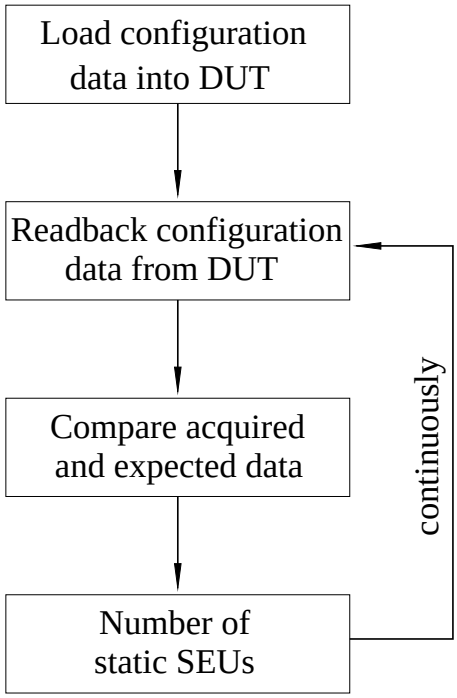

Figure 22: Test routine to investigate static SEU in FPGA chips

5.3.4 Control application

There was developed dedicated software (see Figure 23) in Python language, using Tix/Tkinter libraries for Graphic User Interface.

Figure 23: Control application panel for test system for static SEU in FPGA chips

The application uses Impact software in batch mode from Xilinx ISE development environment to perform programming and reading back configuration data of FPGA chip.

Start button starts the routine to investigate static Single Event Upsets. It is done continuously until the stop button is pressed. All output data from Impact application, run in background, is displayed in program window and can be logged into file.

6 Irradiation experiments

There were performed several experiments with developed test systems. Results are included in this section and discussed.

6.1 Measurements of light attenuation from Light Emitting Diodes

Light reduction was investigated after irradiation of GaAs (Galium Arsenide) Light Emitting Diodes:

- at Hahn-Meitner-Institut (see page 63),
- at superconducting medical cyclotron at Harper University Hospital (see page 64),
- in Linac II tunnel at DESY (see page 62),
- with $^{241}Am/Be$ neutron source (see page 65),

In all experiments we have used 5mm Panasonic LN48YPX GaAs diodes [53]. The colour was chosen to be yellow, because of highest sensivity of photodiode, used in developed photometer.

The light attenuation was evaluated using formula:

$$\text{Attenuation} = \frac{\text{Light output after irradiation}}{\text{Light output before irradiation (control)}} * 100\%$$

6.1.1 Experiments at Hahn-Meitner-Institut

Light Emitting Diodes were irradiated at various gamma dose levels and evaluated thereafter. The light attenuation was assessed. Results are presented in Table 3.

Dose [Gy]	Attenuation [%]
96.3	93
950	90
9810	84
98100	43

Table 3: The results of LEDs radiation experiments with ^{60}Co at Hahn-Meitner-Insitut - light attenuation

6.1.2 Experiments at superconducting medical cyclotron at Harper University Hospital

Light Emitting Diodes were irradiated with various neutron fluxes and then evaluated. The light attenuation was assessed. Results are presented in Table 4.

Neutron fluence $[n/cm^2]$	Attenuation [%]
$1.60 * 10^7$	95
$9.61 * 10^7$	92
$9.93 * 10^8$	91
$1.00 * 10^{11}$	82
$9.81 * 10^{11}$	29

Table 4: The results of LEDs radiation experiments with fast neutrons from superconducting medical cyclotron at Harper University Hospital - light attenuation

6.1.3 Experiments in Linac II tunnel at DESY

There are presented results from two experiments:

- investigations on the spatial distribution of neutrons,
- investigations on neutron shielding using polyethylene.

Experiment on the Spatial distribution of neutrons

Three sets of LEDs were placed in three positions, in the same distance (140cm) from electron/positron converter (inside of Linac II tunnel) - the source of neutron radiation (see Figure 24).

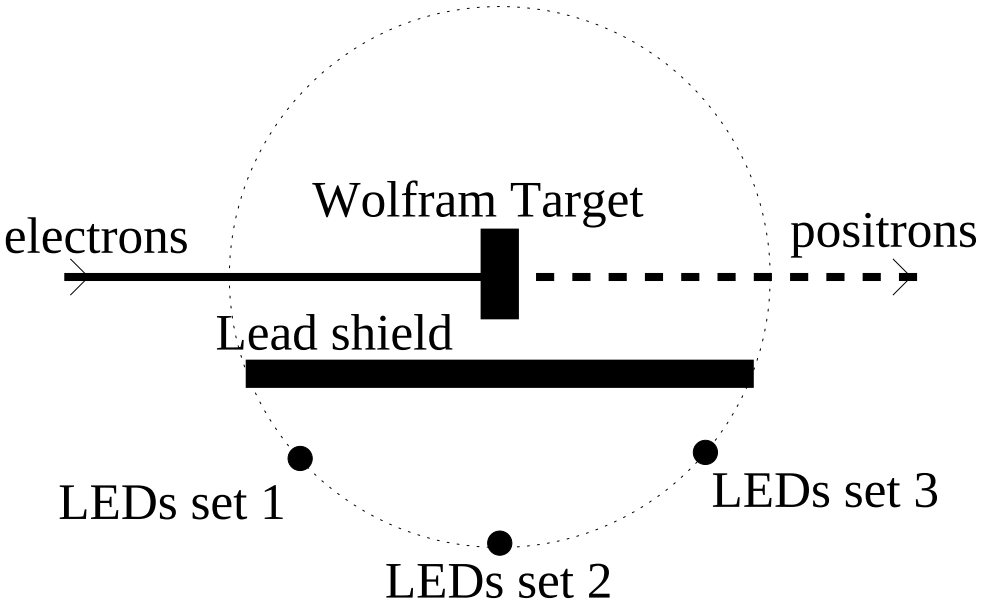

Figure 24: Placement of LEDs sets in neutron spatial distribution experiment in Linac II tunnel

The results of experiment are presented in Table 5. The light output attenuation is almost the same for these three measurement positions. The neutron radiation is isotropic - has the same intensity regardless of the direction of measurement.

Position	Angle from the tube [degree]	Attenuation [%]
1	135	75
2	90	76
3	45	74

Table 5: The results of neutron radiation isotropy experiment with LEDs in Linac II tunnel - light attenuation

Neutrons shielding investigations using polyethylene spheres

Four sets of LEDs were put inside of polyethylene spheres with different radius (polyethylene thickness) (see Figure 25). The spheres were placed in the Linac II tunnel in the same distance from electron/positron converter. One set of LEDs without any shielding was also put in the same position.

Figure 25: Polyethylene spheres for LEDs radiation experiments in Linac II tunnel

After irradiation the light attenuation was assessed. The results are presented in Table 6.

Different values of attenuation for different spheres radius shows that polyethylene absorbes the neutrons (see Figure 26). It can be used as a shielding material for electronic devices against the neutron radiation.

Sphere	radius [cm]	Attenuation [%]
E	3.735	98
D	6.22	97
C	9.8	96
B	12	95
bare	-	83

Table 6: The results of LEDs radiation experiments in Linac II tunnel - light attenuation

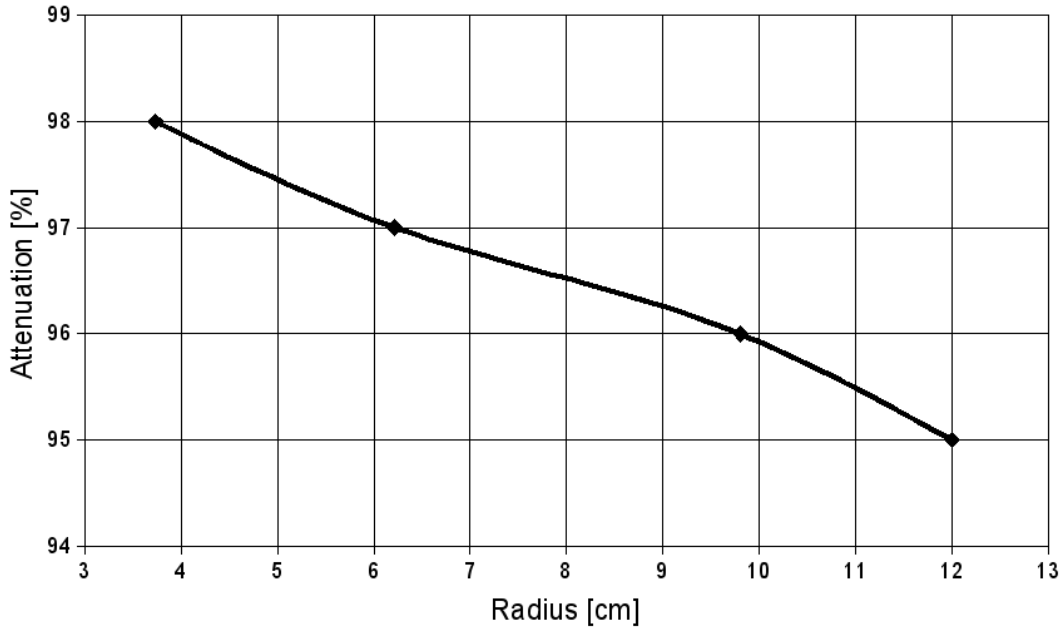

Figure 26: The results of LEDs radiation experiments in Linac II tunnel - light attenuation of photoneutrons in polyethylene

6.1.4 Experiments with $^{241}Am/Be$ neutron source

Sets of LEDs were placed in the same distance from $^{241}Am/Be$ neutron source, but for different times. This varied the neutron doses absorbed by samples.

After neutron irradiation, the light attenuation was assessed. The results are presented in Table 7.

Neutron fluence $[n/cm^2]$	Attenuation [%]
$1.0 * 10^5$	98
$1.0 * 10^5$	97
$1.3 * 10^9$	96
$4.7 * 10^9$	95
$1.2 * 10^{10}$	93
$2.0 * 10^{10}$	90

Table 7: The results of LEDs radiation experiments with neutrons from $^{241}Am/Be$ source - light attenuation

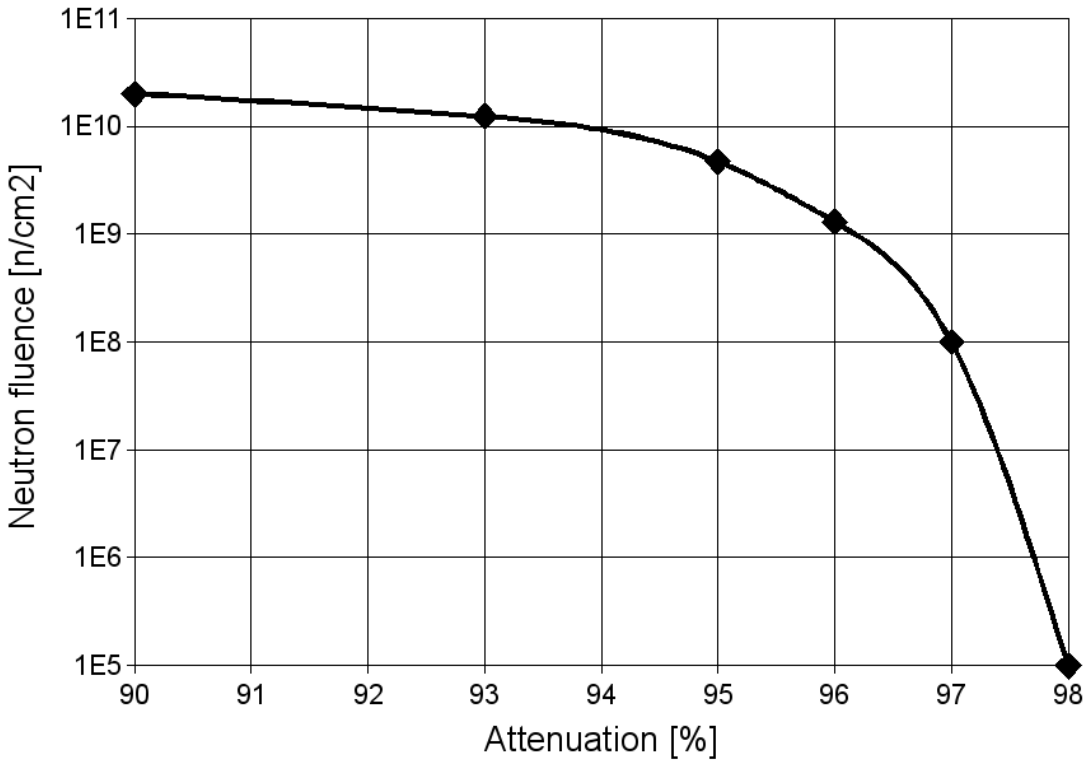

Figure 27: Calibration curve for LEDs irradiated with $^{241}Am/Be$ source

This experiment allows to calibrate Light Emitting Diodes for neutrons from $^{241}Am/Be$ source. The calibration curve is presented on Figure 27.

6.2 Estimation of irradiation effects in semicondutor memories at K130 cyclotron at University of Jyväskylä

Irradiation effects in semiconductor memories were investigated during irradiation at K130 cyclotron at University of Jyväskylä (see page 61).

We have tested folowing types of memories:

- SDRAM - ISSI IS42S16400 (64 Mbits, $0.18\mu m$ technology) [46],
- FLASH - AMD AM29LV160D (16 Mbits, $0.23\mu m$ technology) [45].

6.2.1 FLASH memories

We have tested three chips of FLASH memory. All memories survived the irradiation with beam intensity of $6*10^7 protons/cm^2/s$, up to the dose of $1.2*10^{11} protons/cm^2$, without any errors. Defects appeared during the irradiation with higher beam inensity (see Table 8).

There were only changes from ’0’ to ’1’, not in the other way. That’s because of method of storing data in the FLASH memory cell.

The errors appeared sequentially. First in the four least significant bits of the data word, then in the next eight bits, and so on. At the end, the values of all bits were ’1’. This complete damage of memory appeared after the total doses presented in Table 8. It is highly probable that these errors were a result of dynamic disturption of FLASH memory internal logic. [1][2]

Tests executed a few days after the irradiation experiments, revealed that FLASH memories stored the correct, programmed before data - the errors disappeared, but the erase function was still not working. This was probably caused by destruction of the charge-pump.

Confronting this results with other tests, it can be found that the most susceptible effects of Total Integrated Dose (TID) element in such devices is a charge pump. The memory cell itself is resistant enough and the SEEs during tests are results of SEUs in internal control logic.

# FLASH	First errors		Complete disturption	
	After total dose [$protons/cm^2$]	At beam current [$protons/cm^2/s$]	After total dose [$protons/cm^2$]	At beam current [$protons/cm^2$/s]
FLASH 1	$7.6*10^{11}$	$3.5*10^9$	$8.0*10^{11}$	$3.5*10^9$
FLASH 2	$5.95*10^{11}$	$3.5*10^8$	$6.5*10^{11}$	$3.5*10^8$
FLASH 3	$6.3*10^{11}$	$3.25*10^8$	Not investigated	

Table 8: The results of FLASH memories radiation experiments with proton beam K130 cyclotron at University of Jyväskylä - doses and beam currents for first errors and complete disturption

6.2.2 SDRAM memories

Complete, permanent destruction of memory was not observed. Only bit upsets (Single Event Upsets) appeared, but no stuck bits were detected.

The number of ’0’ to ’1’ upsets was approximately the same as the number of ’1’ to ’0’ upsets.

There were counted crosssections for tested memories:

- SDRAM 1 - $2.4*10^{-9}$ cm^2/device (2237 SEUs),
- SDRAM 2 - $1.6*10^{-9}$ cm^2/device (951 SEs).

Relatively lov values of crosssections may be a consequence of the high frequency of memory refreshing. Capacitors were charged to the proper voltage level so often that ionized particles could not change their potentials. [1][2]

The results are comparable with other made by different laboratories [30][31][32][33].

6.3 Measurements of static Single Event Upsets in FPGA chips

Static Single Event Upsets were investigated during irradiation of FPGA chips:

- at K130 cyclotron at University of Jyväskylä (see page 61),

- in Linac II tunnel at DESY (see page 62),
- in Tesla Test Facility II at DESY (see page 63),
- with $^{241}Am/Be$ neutron source (see page 65).

During experiments at K130 cyclotron at University in Jyväskylä there were used 3 boards Memec Spartan-IIE Development Kits (see Figure 28) [56] with Xilinx Spartan-IIE XC2S300E [55] chip onboard. The rest of irradiation experiments (in Linac II tunnel, in Tesla Test Facility II tunnel, with $^{241}Am/Be$ neutron source) were performed using Memec Virtex-II LC 1000 Development Kit (see Figure 29) [58] with Xilinx XC2V1000 [57] onboard. Characteristics of these devices are presented in Table 9.

Chip	XC2S300	XC2V1000
Technology	$0.18\mu m$	$0.15\mu m$
Power supply	1.8 V	1.5 V
System gates	300,000	1,000,000
Size of configuration bitstream	1,875,648 bits	4,082,592 bits

Table 9: Xilinx Spartan-IIE XC2S300 and Virtex-II XC2V1000 main parameters

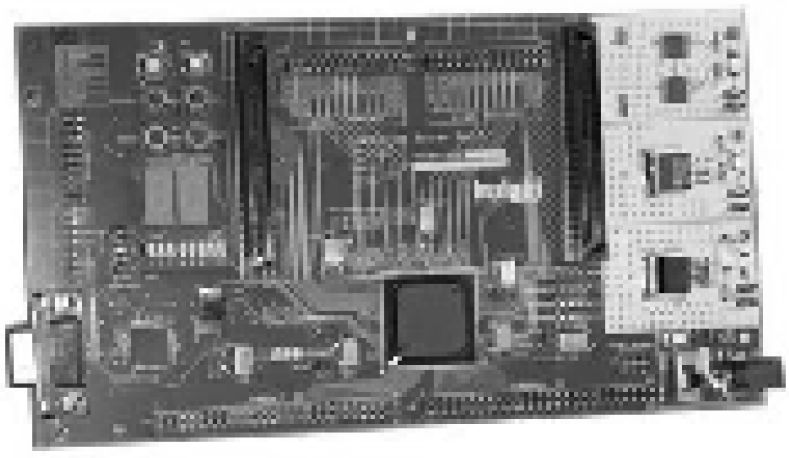

Figure 28: Memec Spartan-IIE Development Kit [56]

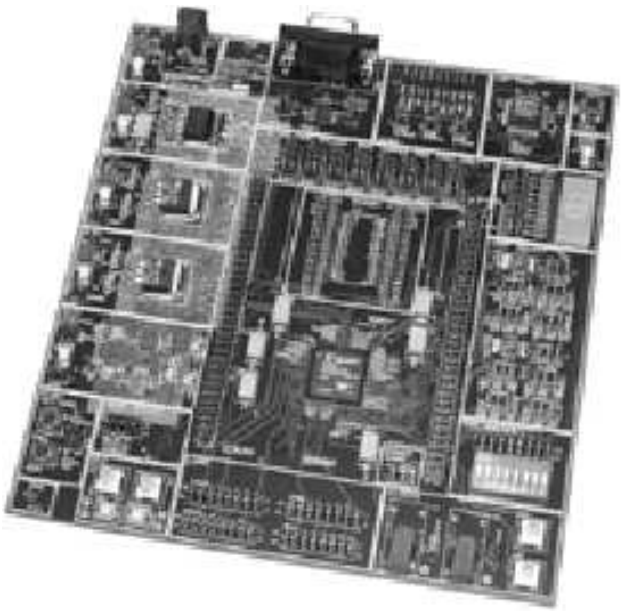

Figure 29: Memec Virtex-II LC 1000 Development Kit [58]

6.3.1 Experiments at K130 cyclotron at University of Jyväskylä

There were no permanent destruction of FPGA chips during irradiation experiments. Only dynamic Single Event Upsets were noticed. Using osciloscope there was attempt to observe dynamic errors, but there were none. Devices worked correctly after taking back from radiation environemnt. The results are presented in Table 10.

Protons energy [MeV]	# FPGA	dose [$1/cm^2$]	SEUs	σ/device [cm^2]	σ/bit [cm^2]
30	FPGA 1	$1.2*10^{12}$	25046	$2.0*10^{-8}$	$1.1*10^{-14}$
	FPGA 2	$2.5*10^{12}$	43859	$1.7*10^{-8}$	$9.3*10^{-15}$
	FPGA 3	$1.6*10^{12}$	29068	$1.9*10^{-8}$	$1.0*10^{-14}$
50	FPGA 3	$3.4*10^{10}$	770	$2.3*10^{-8}$	$1.2*10^{-14}$

Table 10: The results of FPGA radiation experiments with proton beam - SEU crossection

The results of irradiation experiments are very similar to achieved in other laboratories (see Table 11) [38][41][34].

Device	Technology	Protons energy [MeV]	σ/bit [cm^2]
Virtex XCV200	$0.22\mu m, 2.5V$	60	$1.3 * 10^{-14}$
Virtex	$0.22\mu m, 2.5V$	10-100	$2.4 * 10^{-14}$
Virtex E	$0.18\mu m, 1.8V$	10-100	$3.4 * 10^{-14}$
Virtex II	$0.15\mu m, 1.5V$	10-100	$7.5 * 10^{-14}$
Virtex II-Pro	$0.13\mu m, 1.5V$	10-100	$5.3 * 10^{-14}$
Spartan 3	$0.09\mu m, 1.2V$	10-100	$3.3 * 10^{-14}$

Table 11: The results of FPGA radiation experiments with proton beam achieved in other laboratories and experiments - SEU crossections

6.3.2 Experiments in Linac II tunnel at DESY

We have performed radiation experiments on configuration memory (static SEUs) of FPGA in Linac II tunnel. The device was placed near the entry to the tunnel, 20m from electron/positron converter, near the wall. Test was performed for 37 days of operational work of Linac II accelerator. During that time FPGA was programmed once a hour.

The results (number of Single Event Upsets per day and per hour and time before Single Event Upset) are presented on Figures 32, 30 and 31.

Figures 30 and 31 shows that there is not assurance that device survive without any errors for particular time. Time before first SEU after programming can be very short. In such strong radiation field, as is in Linac II tunnel, FPGA should be reprogrammed as often as it is possible.

The Figure 32 shows big dependence of Single Event Upsets number per day from PIA integrated current. That's the confirmation that SEUs are depended on radiation level.

No permanent damages were observed.

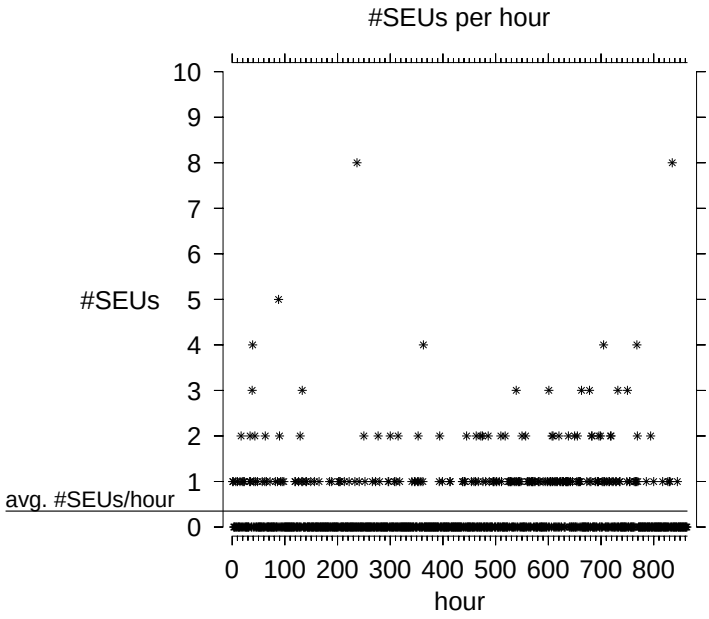

Figure 30: The results of FPGA radiation experiments in Linac II tunnel - Single Event Upsets per hour

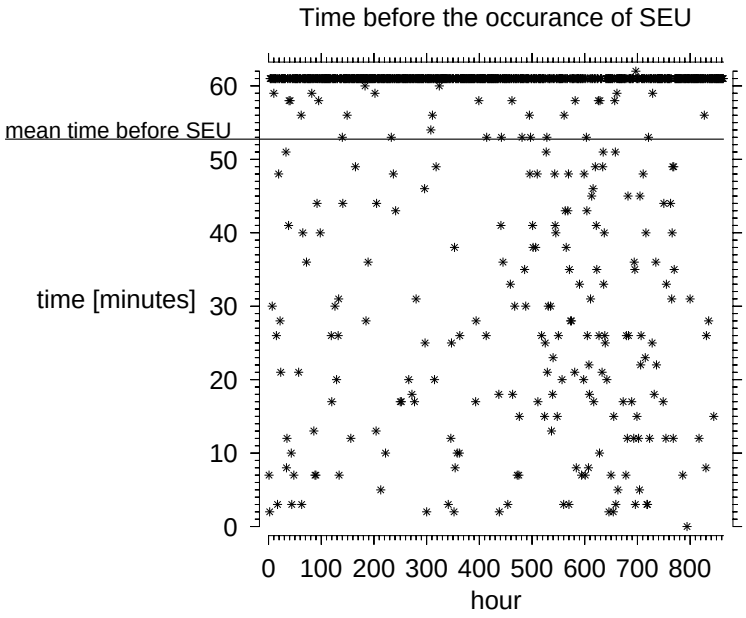

Figure 31: The results of FPGA radiation experiments in Linac II tunnel - Time before occurance of Single Event Upset

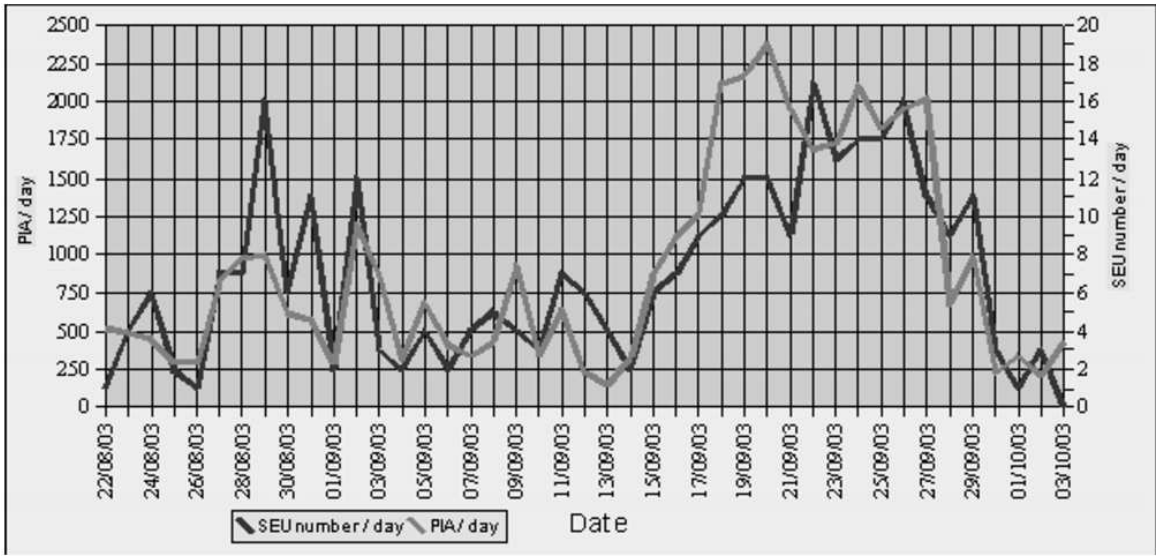

Figure 32: The results of FPGA radiation experiments in Linac II tunnel - Single Event Upsets per day and PIA integrated current per day

6.3.3 Experiments in Tesla Test Facility II tunnel at DESY

We have performed radiation experiments on configuration memory (static SEUs) of FPGA in Tesla Test Facility II tunnel. The device was placed just after first accelerating module, about 2 meters from accelerator tube, near the wall. Test was performed for 42 days of operational work of TTF II accelerator. During that time FPGA was programmed once a day.

The results (number of Single Event Upsets per day and time before Single Event Upset) are presented on Figure 33 and 34.

The avarage number of Single Event Upsets per day during the enitre experiment was about 1 (see Figure 33). It proves that FPGA could work in such environment without any severe problems because of SEUs.

The mean time from programming FPGA to first Single Event Upset during the whole experiment was about 15 hours (see Figure 34). It proves that often refreshing of the FPGA configuration memory prevents it from uncorrect work.

No permanent damages were observed.

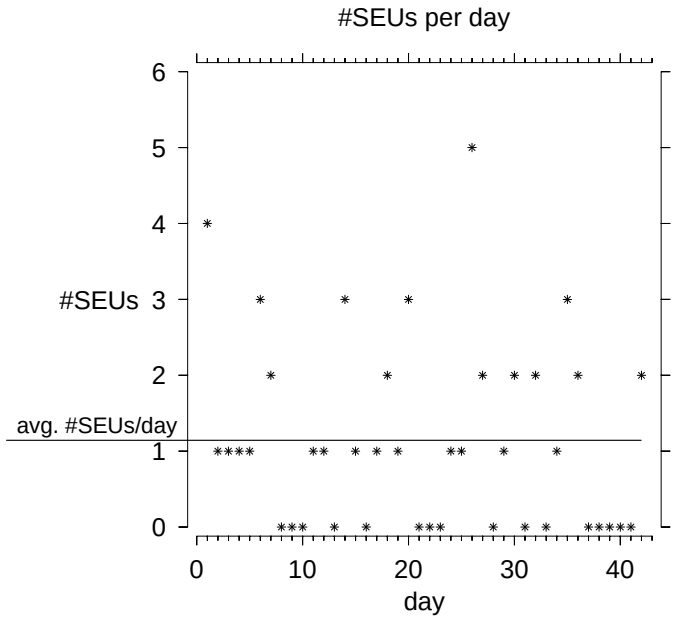

Figure 33: The results of FPGA radiation experiments in Tesla Test Facility II tunnel - Single Event Upsets per day

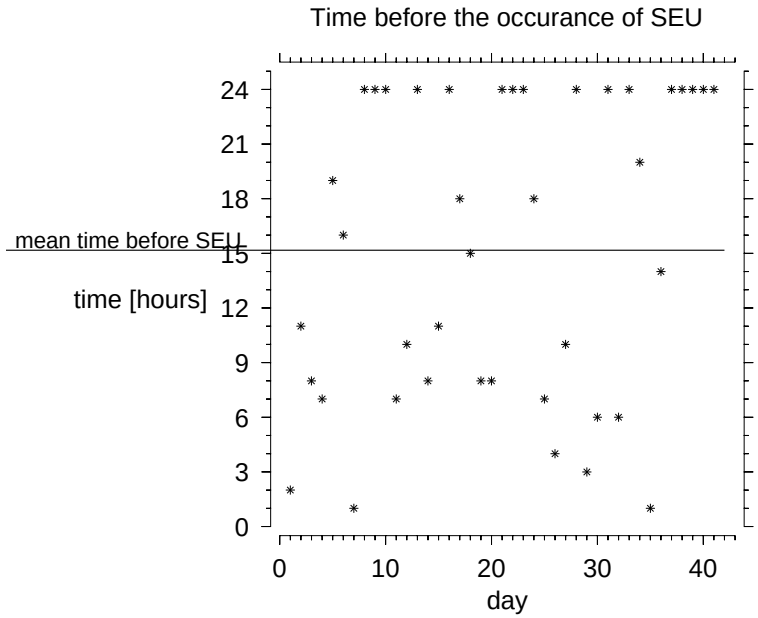

Figure 34: The results of FPGA radiation experiments in Tesla Test Facility II tunnel - Time before occurance of Single Event Upset

6.3.4 Experiments with $^{241}Am/Be$ neutron source

The configuration memory radiation experiments were done, to investigate static Single Event Upsets. The DUT was placed 10 cm away from the $^{241}Am/Be$ neutron source. The results of irradiation runs are presented in Table 12.

No	^{241}Am/Be source	water moderator	time [hours]	# SEUs
1	not present	not present	24	0
2	present	not present	24	9
3	present	present	24	2

Table 12: Results of FPGA irradiation experiments with $^{241}Am/Be$ source

In presence of light water moderator there are smaller number of Single Event Upsets. This moderator slows down the neutrons.

The results achieved in these experiments confirms with experiments presented in other publications [35]:

- small crossection of generation of ionizing particles by thermal neutrons,
- SEUs in FPGA caused mainly by fast neutrons.

7 Conclusions

The experiments presented in this thesis proved the radiation causes damages in electronic devices. There were presented measurement systems to investigate this phenomena in different kinds of components. All developed devices and software worked correctly, aiming the established goals.

Light Emmiting Diodes based fast neutrons dosimeter

The experiments with digital photometer for Commercial-Off-The-Shelf Light Emitting Diodes dosimeter proved that GaAs LEDs are useful as a detectors for fast neutrons. The idea of measuring neutron doses with Light Emitting Diodes introduces new method of dosimetry, which can be very competitve to other techniques, as for example to Thermo Luminescent Dosimeters (TLD). The comparison between TLDs and LEDs is presented in Table 13.

Important features of the dosimetry methods	Neutrons dosimetry using	
	TLDs	LEDs
Device sensivity	High	Low
Read-out method	Indirect, slow	Direct, fast
Cost of the sensor/detector	Low	Very low
Cost of the read-out device	High	Low

Table 13: Comparison of two dosimetry methods (with TLDs and LEDs) for the estimation of fast neutrons dose

The LED-based dosimeter can be useful in many applications:

- neutrons dosimetry for high fluxes (industrial and medical applications),
- fluence monitoring,
- electronic components damage monitorng,
- beam loss monitoring.

The main disadvantage is the necessity of calibrating Light Emitting Diodes for particular neutrons energy and type of used Light Emitting Diodes..

FLASH memories

The test system for semiconductor memories helped to understand that FLASH memories survives high dose before first errors, but the damage cannot be repaired. The experiments provide the informations needed to choose the memories to be used in CMS experiment in CERN. It was decided that FLASH memory is more reliable than SDRAM [1][2].

SDRAM memory and FPGA chips

The main problem in SDRAM memories and in FPGA chips (built in SRAM technology) are Single Event Upsets. There are caused by neutrons. Gamma radiation only limits the lifetime of devices but does not cause improper work.

Experiments proved that radiation mitigation methods should be used to ensure correct work of devices in radiation environment. Some of these techniques are presented in appendix for this thesis (see page 68).

A Irradiation facilities

This section presents the facilities which have been used for radiation investigations, presented in this thesis:

- The K130 cyclotron at University of Jyväskylä (Finland),
- Linac II tunnel at DESY (Hamburg, Germany),
- Tesla Test Facility II tunnel at DESY,
- Hahn-Meitner-Insitut (Berlin, Germany),
- The K100 neutron-therapy cyclotron at Harper University Hospital (Detroit, USA),
- $^{241}Am/Be$ neutron source.

A.1 The K130 cyclotron at University of Jyväskylä (Finland)

The K130 cyclotron is used to accelerate protons (2-75 MeV) and heavy ions. Area of beam illumination is adjustable and beam intensity is measured with the Faraday cup.[28] Devices Under Tests (DUT) are placed in the vacuum chamber (see Figure 35).

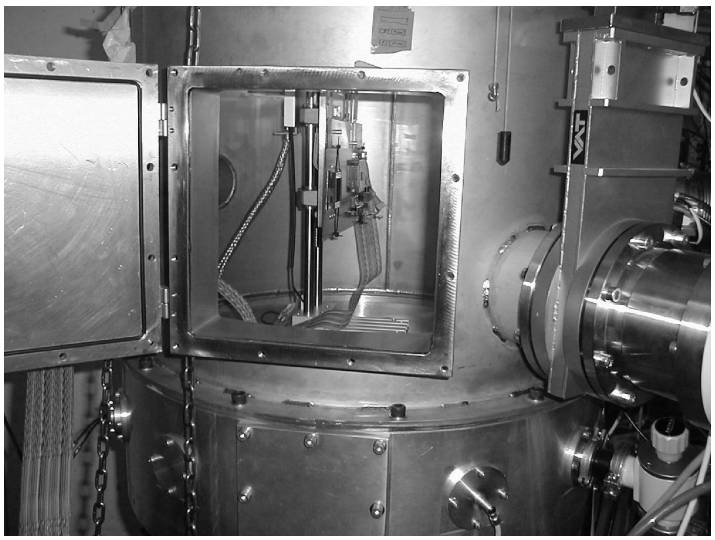

Figure 35: DUT inside vacuum chamber at K130 cyclotron at University of Jyväskylä

A.2 Linac II tunnel at DESY (Hamburg, Germany)

Linac II is DESY's only electron accelerator injecting high energy positrons or electrons (450 MeV) to booster synchrotron DESY II. It consists of two parts (see Figure 36). First one accelerates electrons produced by 150 keV electron source. Electrons with energy about 450 MeV hit the tungsten conversion target and produce electron-positron pairs. There are also neutrons and gamma radiation produced as a parrasistic radiation. The positrons are stored in Positron Intensity Accumulator (PIA), and then delivered to DESY II. [29]

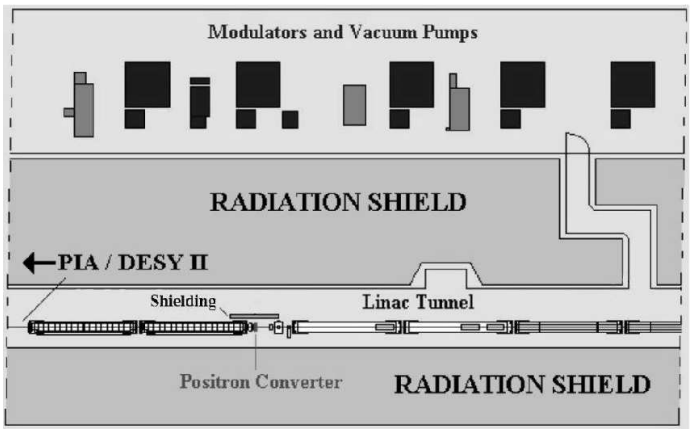

Figure 36: Linac II tunnel

The radiation environment in Linac II tunnel is not well known. The only value which can help quantify it is PIA current. PIA current coresponds to number of electrons hitting the converter and to parasitic radiation. The accumulated PIA current (PIA charge) corresponds to total neutron and gamma dose.

During the irradiation experiments Devices Under Tests (DUT) were placed in various positions along the tunnel (see Figure 36). Changing the distance between the DUT and e^-/e^+ converter allows to change radiation level. Its lowest value is near the entry corridor, about 20 meters away from the target and the highest value is near the converter. It should be pointed that electron-positron converter is placed behind the lead shield. This shielding reduces gamma radiation exposure to personel working in tunnel during the machine maintance, not affects the neutrons.

A.3 Tesla Test Facility II tunnel at DESY (Hamburg, Germany)

TESLA Test Facility II (TTF2) is a test system for TESLA technology and X-FEL experiment at DESY. It's built using the same technology as it will be used for future accelerators.

The DUTs were placed in different locations inside the tunnel (see Figure 37) to vary the radiation level. The experiments were done using unmeasured parasistic radiation during accelerator operation, mainly from cryogenic heatload.

Figure 37: TESLA Test Facility II tunnel

A.4 Hahn-Meitner-Insitut (Berlin, Germany)

At Hahn-Meitner-Institut large area irradiation of devices is possible by using a so called 'panorama' source. Several $30cm$ long ^{60}Co batons provide a radial field with very high intensity and Gamma rays avarage energy about $E_G = 1.25$ MeV during following phenomena:

$$^{60}Co \rightarrow ^{60} Ni* + e^- + \overline{\nu_e}$$

$$^{60}Ni* \rightarrow ^{60} Ni + \gamma$$

The calculated dose rates within a range from $1.6kRad/h$ ($2cm$ from source) to $220Rad/h$ ($17cm$ from source) was achieved.

A.5 The K100 superconducting neutron-therapy cyclotron at Harper University Hospital (Detroit, USA)

This is the first superconducting cyclotron for medicine. It was designed and constructed at the NSCL (National Superconductiong Cyclotron Laboratory) and is now in use for cancer treatment at the Gershenson Radiation Oncology Center at Harper University Hospital in Detroit.

The cyclotron itself accelerates deuterons. Sometimes known as "heavy hydrogen", deuterons differ from normal hydrogen in that they have a neutron as well as a proton in their nucleus. The cyclotron's fast-moving deuterons are stopped in a target of beryllium just before their exit from the cyclotron. This produces a beam of high-energy (30 MeV) neutrons, which is then directed against the cancer patient's tumor (see Figure 38) or could be used for irradiation of electronic devices.

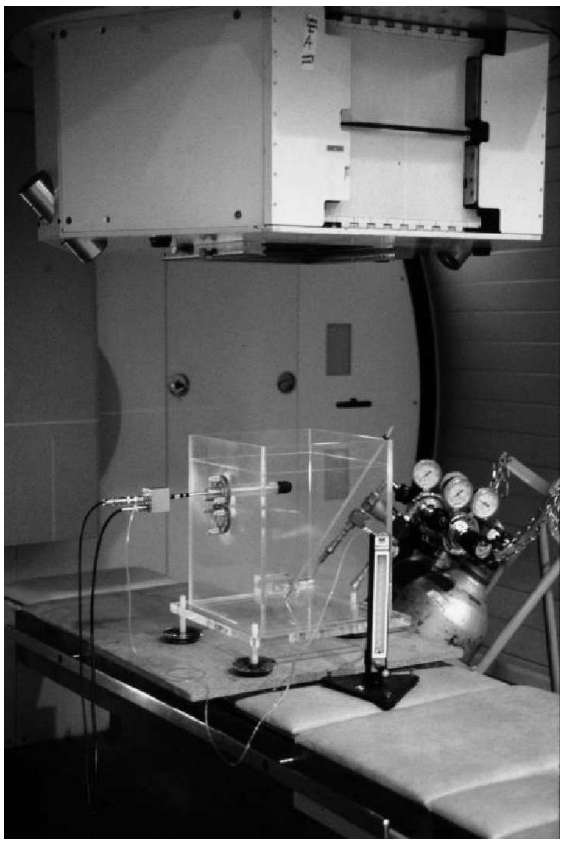

Figure 38: Harper Cyclotron phantom ion chamber for neutron calibration

A.6 $^{241}Am/Be$ neutron source

For the experiments there were used simple neutron irradiation facility with variable avarage energy using a light water moderated $^{241}Am/Be$ source (see Figure 39). The neutron spectrum of this setup is to be very similar to neutron field generated from electrons with energy about 1.6 GeV on niobium material. Niobium is the main constructing material of the TESLA cavities.

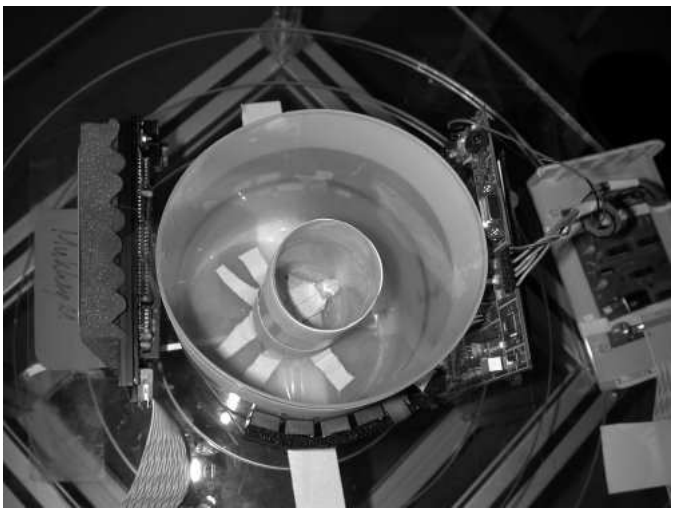

Figure 39: Plastic jar for $^{241}Am/Be$ neutron source and for water moderator

Using light water moderation the average neutron energy drops from 5.1 MeV to 3.3 MeV (for a moderator thickness of 6.5 cm). Maximum of neutron flux moves to low energy[10][26][27].

B Sources of Single Event Upsets

Relatively big charge should be deposited in a small (critical) volume to trigger SEU. Only heavy ions or alpha particles have big enough LET (Linear Energy Transfer) to produce such a big charge. But these particles have very short ramge (below about $10\mu m$), so they have to be produced near the most sensitive area by other particles with higher range (protons or neutrons).

There are different phenomenons producing secondary particles by neutrons or protons in the silicon [1][38]:

- Generation by high-energy hadrons ($E > 20MeV$).

  High-energy hadrons interact inelasticly with silicon nucleons producing the nuclear recoils (see Figure 40):

$$p(n) + Si \rightarrow \text{nuclear recoils} + ...$$

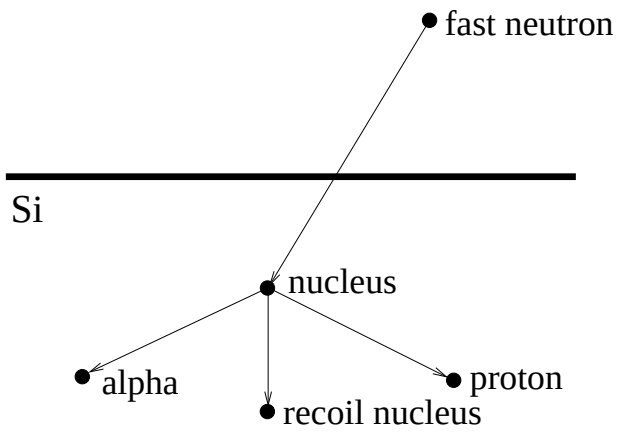

Figure 40: Generation of secondary particles by high-energy hadron (here: fast neutron)

- Generation by neutrons below $20Mev$.

  The low energy neutrons interacts with silicon nucleons mainly elasticly:

$$n + Si \rightarrow n + \text{recoiled } Si$$

- Generation by thermal neutrons.

  Thermal neutrons produce alpha particles in ${}^{10}B(n_{th},\alpha)^{7}Li$ phenomenon (see Figure 41):

$$ {}^{10}B + n \rightarrow {}^{7}Li + \alpha + \gamma $$

  Boron is a common dopant in the technology of ICs manufacture.

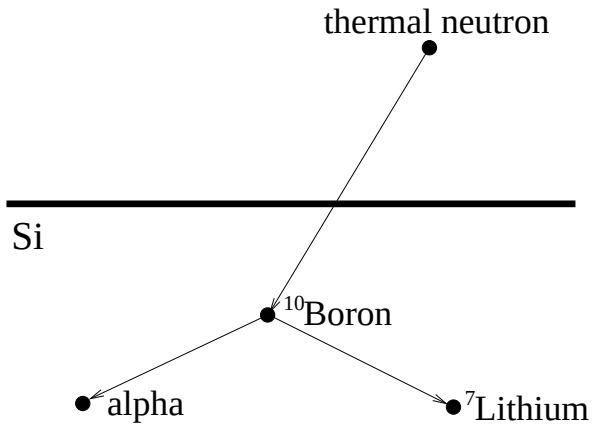

Figure 41: Generation of secondary particles by thermal neutrons in ${}^{10}B(n_{th},\alpha)^{7}Li$ phenomenon

C Overview on radiation mitigation techniques

Presented in this thesis experiments show the electronic devices suffer because of irradiation. To warrant proper work there are several radiation mitigation techniques:

- conventional shieldings,
- chips dedicated to work in irradiation environment,
- appropriate system design.

These ideas and methods are briefly discussed below. There are presented in details in other publications, eg. [20][39][40][41][42][43].

C.1 Conventional shieldings

The most important shielding is against gamma radiation. Neutrons for electronic devices is not a critical problem. They cause only not-permanent errors. Shielding against neutron radiation is less important.

Let us consider that the estimated maximum value of gamma radiation is about 10 rad / h = about 10^6 rad / 20 years (as it's predicted for ILC). The maximum Total Ionizing Dose for electronic devices is about a few krads. In this case gamma field should be reduced to 0.1 % to secure in-tunnel electronics. The best substance for this purpose is concrete. This material has HVL factor about 100 mm, for gamma radiation energy 5 MeV. Half-Value Layer (HVL) is the thickness of material to reduce gamma radiation to half [23]. To reduce gamma to 0.1 % there should be used $10 * 100mm = 1m$ of concrete wall.

C.2 Components dedicated to radiation environment

Some companies produce chips designed to work in high radiation environment. For example it could be XQR family of Xilinx FPGA chips (see Table 14. It has bigger (200 krads instead of tens krad) Total Ionizing Dose. This chips have longer lifetime exposed to high radiation.

There are also whole electronic systems dedicated to radiation environment. Maxwell company produces SCS750 board which includes 3 PowerPC on it (see Table 15). In comparison to commercial PowerPC it can withstand a dose in excess of 100 krad. It has also incredible high SEU rate ($< 9 * 10^{-6}$ upset per day on GEO orbit).

	Virtex-II (XC2V1000)	Virtex-II Q-Pro (XQR2V1000)
Technology	0.15 μm	0.15 μm
Number of system gates	1M	1M
Voltage supply	1.5 V	1.5 V
SEU rate		$< 1.5 * 10^{-6}$ upset/day (on GEO orbit)
TID	ab. tens krad (Si)	> 200 krad (Si)
Price	ab. 250 €	ab. 3500 €

Table 14: Comparison of commercial (Virtex-II) and rad-hardned (Virtex-II Q-Pro) FPGA chips

	Force Computers CPU-56	Maxwell SCS750
CPU	UltraSPARC-III+ 650MHz	3 * PowerPC 750FX with TMR in radhard FPGA
SDRAM	512MBytes ECC-Protected	256MBytes Reed-Solomon Protected
SEU rate		$< 9 * 10^{-6}$ upset/day (on GEO orbit)
TID	ab. few krad (Si)	> 100 krad (Si)
Price	ab. 5000 €	ab. 10000 €

Table 15: Comparison of commercial (Force Computers CPU-56) and rad-hardned (Maxwell SCS750) computers

These examples don't fullfil the market but there are good to show that the main disadvantage of rad-hard devices is the price (see Tables 14 and 15). It is even few times higher than price of normal, Commercial-Off-The-Shelf devices.

C.3 Appropriate system design

There are some methods to mitigate irradiation problems with electronic devices in earliest - designing stage. For example designer could use:

- cold redundancy (againsts problems with TID) [19][20],
- current Limiting (againsts problems with SEL, SEB) [19][20],
- software and hardware error detection and correction (againsts problems with SEU) [19][20],
- constant refreshing (againsts problems with SEU) [19][20],
- hot redundancy triple voting (againsts problems with SEU) [19][20][39][43].

D Overview on radiation safety

Experiments presented in this thesis were performed in irradiation environment, which is very hazardous to human health. Because of strict health safety regulations, the author had to obide by many restrictions, including the participation in radiation safety course every year.

The main safety rules are presented in this section. Thery are based on radiation protection instructions at DESY [24], and compying with international standards.

D.1 Authorities responsible for radiation protection

Every institute working with radiation has its own Radiation Protection Department. People working there (Radiation Safety Officers) are specialized to take care about radiation protection of other employees of the institute. In principle, they are responsible for:

- organising annual radiation safety courses,
- local dose measurements,
- personal dose measurements and monitoring these doses,
- reporting the exposure incidences.

D.2 Personal protection

The avarage background radiation dose for person per calender year is about $1mSv$. People, who may be exposed to higher dose, are regarded as occupationally radiation exposed persons. There are divided into two categories:

- category A - occupational health screening is necessary,
- category B - occupational health screening is not necessary.

Author of this thesis is consider as occupationally radiation-exposed person in category B. The maximum permissible doses are presented in Table 16.

Category	Dose
category A occupationally radiation-exposed persons	20mSv per calendar year
category B occupationally radiation-exposed persons	6mSv per calendar year
persons not occupationally radiation-exposed	1mSv per calendar year
pregnant women	1mSv during pregnancy
persons under the age of 18	1mSv per calendar year
occupationally radiation-exposed persons	400mSv dose throughout working life

Table 16: Maximum permissible personal doses

D.3 Radiation areas

Regarding local dose rates there are two types of radiation areas:

- Prohibited area - areas in which the local dose rate may exceed $3mSv/h$. If a local dose rate much higher can occur as a result of the operation of an accelerator, it must be secured by an interlock system. Access to a prohibited are is not allowed. Exceptions may be granted by a Radiation Safety Officer.
- Controlled area - area in which persons could receive an effective dose of more than $6mSv$ per calendar year (it corresponds to the maximum local dose rate of $3\mu Sv/h$). Controlled areas may only be entered if the following points are observed:
  - before entering persons must receive instructions,
  - persons enetring area must be equipped with the correst dosimeters,
  - area may only be entered in order to carry out the necessary work,
  - eating, drinking and smoking is not permitted.

List of Figures

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Irradiation effects

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Radiation tests of CMS RPC muon trigger electronic components

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Abstract

The results of proton irradiation test of electronic devices, selected for the RPC trigger electronic system of the CMS detector, will be presented. For Xilinx Spartan-IIE FPGA the cross-section for Single Event Upsets (SEUs) in configuration bits was measured. The dynamic SEUs in flip-flops were also investigated, but not observed. For the FLASH memories no single upsets were detected. Only after irradiating with a huge dose permanent damages of devices were observed. For Synchronous Dynamic Random Access Memory (SDRAM), the SEU cross-section was measured.

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Keywords: FPGA; SRAM; SDRAM; FLASH; SEU; Radiation

1. Introduction

RPC muon trigger system (Pattern Comparator Trigger) is a part of the CMS detector level one (LV1) trigger [1]. Its task is to identify muons, measure their transverse momenta, and determine the bunch crossings from which they originate. The signals from the Resistive Plate Chambers

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(RPCs) are electrically transmitted to the Link Boards (LBs), where they are synchronized, multiplexed, serialized and then sent via optical links to the CMS counting room, where the trigger decision is taken. Most of the LBs will be placed in the crates on the CMS detector balconies in the UXC55 experimental hall cavern (1568 pieces). The boards for RE1/1 RPCs will be placed on the endcap nose, between muon station ME1/1 and hadron calorimeter HE/1 (72 pieces) (Fig. 1). Each set of 16 LBs placed in one crate will be steered by two Control Boards (CBs). The LBs and CBs will have to work in the radiation field, composed mainly of thermal neutrons and high-energy hadrons ($E = 10 - 100$ MeV) [2,3]. The most important electronic devices used on these boards are FPGA chips and memories that store the FPGAs configuration data. The goal of radiation tests was to predict the behaviour of these devices in the radiation environment, select among different types of devices (Synchronous Dynamic Random Access Memory (SDRAM) vs. FLASH memories, Xilinx vs. Altera FPGAs), and to quantify the methods of mitigating the errors.

2. Radiation environment in CMS

The fluxes and spectra of the particles, known from simulation [2,3], are presented in Table 1 (for regions of CMS detector, where boxes with LBs and CBs will be placed). It should be mentioned, that these flux values are not known precisely. There is a factor of two uncertainties in the simulation of flux.

Although the majority of particles are low-energy neutrons, the high-energy ($E > 20$ MeV) hadrons (mainly protons and neutrons) are considered to be the main source of radiation effects in electronic devices in CMS [2,5]. The flux of high-energy neutrons is almost one hundred times bigger than the flux of high-energy protons. From the point of view of the influence on the electronic devices, however, high-energy neutrons are very similar to protons. At these energies the most

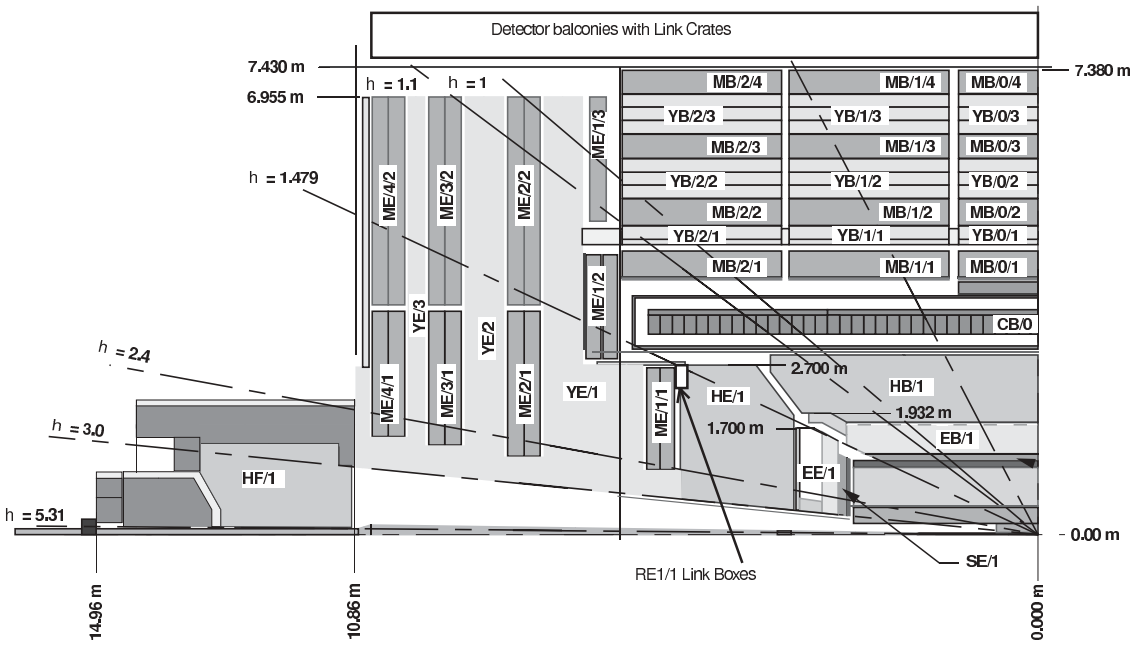

Fig. 1. The cross-section of one quarter of CMS detector. *M****—muon station with RPC detectors.

Table 1
Particle fluxes in regions of CMS detector where link crates will be placed

Particle type	ME1/1 [3] (cm^2/s)	Cavern above endcap [2] (cm^2/s)
Charged hadrons (protons) ($E=10-100$ MeV)	3.6×10^1	1.6
Neutrons $E>20$ MeV	1.1×10^3	84
Neutrons $E=2$–20 MeV	7.2×10^2	93
Neutrons $E>100$ keV	4.4×10^3	370
Neutrons $E<100$ keV	1.1×10^4	650
Neutrons total	1.7×10^4	1100

important are strong interactions with nucleons, while direct ionization is less important. Therefore, proton beam tests of radiation effects give a very good prediction of the influence of the high-energy neutrons on the electronic components in the CMS.

3. Single Event Upsets (SEU) in SRAM-based FPGAs

Static Random Access Memory (SRAM) cells and flip-flops are the two most important components of a FPGA chip where radiation failures occur. These elements can be found e.g. in the logic cell—the basic building block of the tested Xilinx Spartan-IIE FPGA. A logic cell contains a 4-input look-up table, carry logic and one flip-flop. The look-up table is a generator of 4 bits input, 1 bit output logic function and consists of 16 cells of SRAM. The output from a look-up table can be connected to the output of the logic cell either directly or through the D input of the flip-flop. In the latter case, the flip-flop works as a latch, i.e. it synchronizes the output of a look-up table with the clock. The flip-flops are also commonly used for building the counters and shift registers. Two logic cells form a slice, and two slices with additional multiplexers form a configurable logic block. Each configurable logic block is programmed by several dozens of bits stored in SRAM cells [4].

The SRAMs also configure the interconnections between configurable logic block and the I/O logic (definition of pins for input or output, etc.). Usually in FPGA there are also the large blocks of SRAM that can be used as synchronous dual-port memories.

The tested device—Spartan-IIE XC2S300E—has 1,875,648 configuration bits, among them only 98,304 are in look-up tables and 64K in block RAM.

Single Event Upset (SEU) is a change of the logic state of an element storing one bit caused by radiation. Two types of SEUs may be distinguished:

- static SEUs—changes in the configuration bits,
- dynamic (or transient) SEUs—changes in the logic state of the bits, which are supposed to change during normal operation (for example flip-flops).

SEUs affect the performance of FPGA in different ways. Changing the state of one flip-flop working as a latch results in a false value of one bit during one clock period only, while changing the state of one SRAM cell in the look-up table results in a permanent wrong answer for one combination of input bits. Changing the state of one SRAM that programs the interconnection between logic blocks can seriously modify the performance of the whole circuit.

Detailed considerations about the mechanism of SEU in a SRAM cell may be found in Ref. [5]. The main conclusion is that an ionizing particle should deposit a relatively large charge in a small volume to trigger a SEU. Only heavy ions or alpha particles have large enough linear energy transfer (LET) to produce such a big charge. But these particles have a very short range (typically below 10 μm), so they have to be produced inside the chip by other particles with higher range, like protons or neutrons.

In the case of the CMS detector, the high-energy ($E>20$ MeV) hadrons (protons and neutrons) are considered to be the main source of SEUs [2,5]. They can produce nuclear recoils with energies up to 10 MeV and atomic number (Z) usually at least 10 in inelastic interactions with silicon nuclei. These nuclear recoils can easily produce charges needed to trigger a SEU. The expected dependence

of the SEU cross-section on the hadron energy is rather weak (for hadrons energies $>\sim$50 MeV) [2].

Another important conclusion of Ref. [5] is that devices made in modern technologies with smaller integration scales and lower supply voltages are more vulnerable to SEUs, then those made in the past.

4. Radiation-induced errors in FLASH memories

FLASH memories use transistors with a floating gate to store data. Operation of this transistor is based on the Fowler–Nordheim tunnelling of charge carriers from a source (drain) through the oxide to the floating gate. The writing operation injects electrons into the floating gate through the oxide, and the erasing operation removes them from the floating gate. During erasing all bits are set to '1'. The writing operation sets the bits to '0', thus the writing can be done only after erasing [6]. Voltages required for writing and erasing operations (+12, +7 and –9 V), which are higher than the power supply voltage, are provided by the charge-pump circuit. A degradation of this charge-pump is very probable in a radiation environment, because the circuit works with relatively high voltages [7–10].

Ionizing radiation can destroy the isolator structure, allowing the charge accumulated in the floating gate to migrate out of it. In this case, the cell changes its state from '0' to '1'. There is no mechanism changing the state of a memory cell from '1' to '0'.

In the FLASH memories there are also several registers and some logic, controlling the memory, which are vulnerable to radiation.

5. Radiation-inducted errors in SDRAM

Synchronous Dynamic Random Access Memory (SDRAM) uses a capacitor as a data storage element and a transistor as a switch. When the potential of the capacitor is at ground level, the state of the cell is '0'. When this potential is equal to the supply voltage, the state of the cell is '1'.

In a radiation environment, ionizing particles passing through the capacitor generate electron-hole pairs. The potential on the capacitor may then change, changing the memory state. This type of errors—SEUs—are the most frequent errors in SDRAMs [11]. Two types of SEUs can be observed:

- recoverable bit upsets (single or multiple errors in one memory word)
- stuck bits—bits, which do not change their state even after reprogramming.

6. Tests method and results

The tests were performed at the cyclotron in Jyväskylä Accelerator Laboratory, Finland. Two sets of tests were made: first with 30 MeV protons, and then with 50 MeV protons. The beam illuminated an area of 6.25 cm^2 in the first case, and 25 cm^2 in the second one. The homogeneity of the particle flux was assured by "wobblers" which vibrated the beam vertically and horizontally. The beam intensity was measured with a Faraday cup, the measured current was recorded every second. The boards with tested devices were placed in the vacuum chamber.

6.1. FPGA tests

The tested device was Xilinx Spartan-IIE (XC2S300E), made in 0.18 μm technology, supplied with 1.8 V, containing 6912 logic cells and 1,875,648 configuration bits. Read back and verification of the configuration bits are implemented. The tested chip was placed on the Memec Spartan-IIE Development Kit board and was programmed by the JTAG interface.

Two kinds of tests were performed:

6.1.1. Test with read back

The goal of this test was to find the cross-section for SEU in configuration SRAM cells. The device was loaded, and during the irradiation the configuration bits were read back every minute and compared with loaded ones. The number of upset bits was recorded. The results of this test are presented in Table 2. The uncertainty of the

Table 2
The results of SEU test in configuration bits. The uncertainty of obtained cross-section is about 10%

Beam energy	Chip	dose (1/cm^2)	SEUs number	σ/device (cm^2)	σ/bit (cm^2)
30 MeV	FPGA 1	1.2×10^{12}	25,046	2.0×10^{-8}	1.1×10^{-14}
	FPGA 2	2.5×10^{12}	43,859	1.7×10^{-8}	9.3×10^{-15}
	FPGA 3	1.6×10^{12}	29,068	1.9×10^{-8}	1.0×10^{-14}
50 MeV	FPGA 3	3.4×10^{10}	770	2.3×10^{-8}	1.2×10^{-14}

obtained cross-section we estimate at about 10%. The main contribution to this uncertainty comes from the uncertainty of measurement of the proton flux. The statistical error of the number of SEUs is negligible, because of a big number (order of thousands) of observed upsets.

6.1.2. Test of dedicated logic

The goal of this test was to measure the cross-section for dynamic SEU in flip-flops, and to assess the vulnerability of the design to the errors in configuration bits. The FPGA was configured with a 5504 bits shift register (Fig. 2). The input of the shift register was driven by repeating a pattern of four '0' followed by four '1'. The XOR gate compared output of the register with input and indicated the errors. The implemented shift register utilized about 90% of FPGA resources. The outputs of the register and the XOR gate were observed on the scope (Fig. 3).

The test procedure was as follows:

- The tested FPGA was loaded with configuration data. After that the chip started its operation.
- Immediately after loading, the read back of configuration bits was initiated (this function runs in the background, and does not affect the performance of the FPGA). The number of upsets was recorded.
- When the signals on the scope indicated a permanent corruption of the design (Fig. 3), the second read back of configuration bits was initiated. The number of upsets was recorded.

The beam was set at a very low intensity ($\sim 7.5 \times 10^6$ p/cm^2/s), and induced only a few SEUs of the configuration bits per minute. The programming took about 10 s, and could be done with the beam on, because only single error might have occurred during programming time. These errors usually did not affect the chip operation.

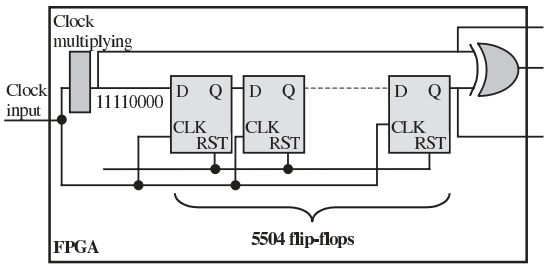

Fig. 2. The schema of the shift register design used for testing the dynamic SEU.

Tests were performed with two different frequencies of FPGA clock: 24 MHz and 100 MHz. In both cases no dynamic SEUs were observed. Fig. 4 presents the distribution of SEUs number in configuration bits after detecting the shift register break.

In several cases, we observed that after a few successive reprogrammings of the FPGA the output of the shift register was stuck in the same, wrong state, in spite of the read back showing '0' or single error. Turning off the power restored the functionality of the chip. This phenomenon was observed 4 times during the test at 24 MHz and 3 times during the test at 100 MHz.

6.2. Tests of memories

Two types of memory have been tested:

- FLASH memories—AMD AM29LV160D (16Mbits)—3 chips
- SDRAM memories—ISSI IS42S16400 (64Mbits, 0.18 μm, 3.3 V)—2 chips

Fig. 3. Performance of the shift register design observed on the scope. Upper signal—the output of the XOR gate, bottom signal—the output of the shift register: (a) normal operation, (b) expected dynamic SEU signal, (c) the shift register is broken off, the functionality of the design is changed, (d) the shift register is broken off, input of the remained rearmost part of the register is connected to '0'.

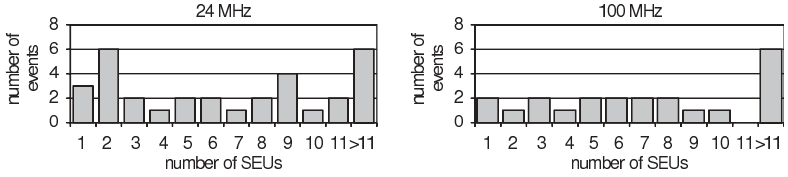

Fig. 4. Number of SEUs in configuration bits after detecting the shift-register breaking. Results of two tests with different frequencies of FPGA clock.

The experiments were performed using the dedicated printed circuit board. The board contained a AVR microcontroller, Altera FPGA, SDRAM memory chip and a ZIF pocket for removable FLASH memory, and provided connections to a PC by RS 232 C and JTAG ports.

The FPGA chip (Altera ACEX 1K EP1K100FC256) was used to implement memory

controllers. The AVR microcontroller (AT90S8515) was used for executing tests of memory and reporting errors to a PC by a serial port. The PC was running appropriate software to control test routines and to configure AVR and FPGA.

Memories were tested dynamically. The whole memory was filled with 16 bits words of pseudo-random values. During the irradiation, read back of data, stored in memory, was performed. The reading phase was repeated consecutively many times. In the SDRAM, word with corrupted data was rewritten immediately after detecting the error. For SDRAM memories auto refresh with a frequency of 2.4 kHz was performed. Several measurements with different beam intensities were carried out.

6.2.1. Results of tests of FLASH memories

All tested memories survived the irradiation with beam intensity of 6×10^7 protons/cm^2/s, up to the dose of 1.2×10^{11} protons/cm^2, without any errors. Errors appeared during the irradiation with higher beam intensity (Table 3). Only changes from '0' to '1', not from '1' to '0' occurred. Errors appeared sequentially, first in the four least significant bits of the data word, then in the next eight bits, and so on. At the end, the value of all bits was '1'. This complete damage of memory appeared after the total doses presented in Table 3. It is highly probable that these errors were a result of dynamic destruction of FLASH memory internal logic. Without complete information from the manufacturer it is hard to prove this conjecture.

In case of FLASH chip number 3 the beam was turned off after registering the first errors. The number of errors increased a bit more, and then started to decrease from 337,939 to 68 wrong bits after 1 h.

Tests executed a few days after the irradiation experiments, revealed that FLASH memories stored the correct, programmed data—the errors disappeared, but the erase function was still not working. This was probably caused by destruction of the charge-pump.

6.2.2. Results of tests of SDRAM

Complete, permanent destruction of memory was not observed. Only bit upsets appeared, but no stuck bits were detected.

There was one test with a large number of writing errors. These errors were reported when the AVR controller read out corrupted data and tried to rewrite them with correct values, but the bits were still not correct. It means that the stuck bits might have occurred, but more probably, the AVR or the control FPGA was corrupted by a dynamic SEU caused by secondary particles.

The number of '0' to '1' upsets was approximately the same as the number of '1' to '0' upsets. For SDRAM chip number 2 there were about 20% of errors with multiple bits flips in one word.

The SEU cross-sections for these memories are:

- SDRAM 1—2.4×10^{-9} cm^2/device (2237 SEUs observed),
- SDRAM 2—1.6×10^{-9} cm^2/device (951 SEUs observed).

We estimate the uncertainty of obtained results at about 10%. Relatively low values of cross-sections may be a consequence of the high frequency of memory refresh. Capacitors were charged to the proper voltage level so often that ionized particles could not change their potentials.

Table 3
Doses and beam currents for errors in FLASH memories

	First errors		Complete damage	
	After total dose (protons/cm^2)	At beam current (protons/cm^2/s)	After total dose (protons/cm^2)	At beam current (protons/cm^2/s)
FLASH 1	7.6×10^{11}	$\sim 3.5 \times 10^9$	8.0×10^{11}	$\sim 3.5 \times 10^9$
FLASH 2	5.95×10^{11}	$\sim 3.5 \times 10^8$	6.5×10^{11}	$\sim 3.5 \times 10^8$
FLASH 3	6.3×10^{11}	$\sim 3.25 \times 10^8$	Not observed	

7. Conclusions

Although during the FPGAs test no dynamic SEU were observed, it does not mean that such errors could not appear in this type of chip. Rather it indicates, that dynamic SEUs are much less probable then SEUs in the configuration bits.

The second important conclusion is that even a few upsets in configuration bits may corrupt the design, because most of the configuration bits are needed to program the interconnections between the elements of FPGA.

Results obtained from the tests enabled us to estimate the expected SEUs rate induced by high-energy hadrons in the CMS experiment. In the final application, each LB will contain one XC2S400E chip with 2,693,440 configuration bits, ~1.4 times more than in the tested XC2S300E device. In the calculations we took the largest measured cross-section (Table 2) ($\sigma_{SEU} = 2.3 \times 10^{-8}\,cm^2$/device) multiplied by 1.4.

To avoid the accumulation of SEU, all LB FPGAs will be regularly reloaded. The planned reloading time interval T is 10 min. The probability that after time T there will be at least one SEU on one LB can be derived from the Poisson distribution:

$$P_{LB} = 1 - \mathscr{P}(0) = 1 - \exp(-\sigma_{LB}\varphi T)$$

where σ_{LB} is the SEU cross-section of one LB ($\sigma_{LB} = 3.3 \times 10^{-8}\,cm^2$). Taking the particle fluxes from Table 1 (total charged hadrons and high-energy neutrons) one gets:

- in ME1/1 region ($\varphi = 1.2 \times 10^3\,1/cm^2/s$): $P_{LB} = 0.023$,
- on balconies on the detector ($\varphi = 1.0 \times 10^2\,1/cm^2/s$): $P_{LB} = 0.002$.

The link system will consists of 72 LBs in the ME1/1 region and 1568 LBs on the balconies. The probability that after time T there will be k LBs with SEUs is given by the binomial distribution:

$$\mathscr{B}(k, n, P_{LB}) = \binom{n}{k} P_{LB}^k (1 - P_{LB})^{n-k}$$

where n is the number of LB (Fig. 5). The mean of this distribution:

$$\langle k \rangle = nP_{LB}$$

gives an average number of LBs that after time T will have at least one SEU. The corresponding values are:

- in the ME1/1 region—1.7 LBs,
- on the balconies—3.1 LBs.

It is also interesting to calculate the average number of LBs with SEUs. To do this, one has to average P_{LB} over the time T in the formula for $\langle k \rangle$. Since the factor $\sigma_{LB}\varphi T$ in the formula for P_{LB} is very small, P_{LB} depends almost linearly on T. This gives $\langle P_{LB} \rangle \cong P_{LB}/2$, and the average number of LBs with SEUs in time T is two times smaller than $\langle k \rangle$ after time T. Thus the average fraction of the link system affected by SEUs is 0.3%.

Tests proved that FLASH memories are resistant enough to high-energy hadrons. They survived the dose that exceeds a few times the expected dose in ME1/1 region of CMS (expected integrated 10-years fluence in the ME1/1 region is $5.7 \times 10^{10}\,cm^{-2}$) without any errors. The FLASH memories will be used on the CBs.

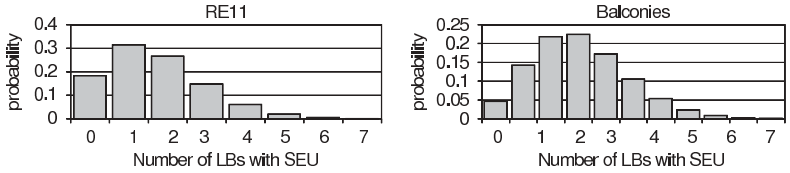

Fig. 5. The expected probability distribution of the number of LB with at least one SEU after 10 min of operation in CMS radiation field. Results for 72 LBs from ME1/1 region and 1568 LBs on balconies.

Table 4
The results of similar tests of FPGAs. The proton cross-section for SEUs in configuration bits for different families of Xilinx devices

No.	Device	Technology [(μm), (V)]	σ/bit (cm^2)	Protons energy (MeV)	References
1	XC4036XLA	0.35, 3.3	0.4×10^{-14}	20–100	[15]
2	Virtex XCV200	0.22, 2.5	1.25×10^{-14}	60	[14]
3	Virtex	0.22, 2.5	2.4×10^{-14}	10–100	[12,13]
4	Virtex E	0.18, 1.8	3.4×10^{-14}	10–100	[12]
5	Virtex II	0.15, 1.5	7.5×10^{-14}	10–100	[12]
6	Virtex II-Pro	0.13, 1.5	5.3×10^{-14}	10–100	[12]
7	Spartan 3	0.09, 1.2	3.3×10^{-14}	10–100	[12]

8. Comparison with results of other tests

Table 4 contains the measured proton cross-section for SEUs in configuration bits for different families of Xilinx devices. It is astonishing that the results from Ref. [12] differ so much from other results: the result no. 3 for Virtex is almost 2 times larger than the result no. 2 presented in Ref. [14]. The result no. 4 for Virtex E is 3 times larger than our result for Spartan IIE made in the same technology. The differences of the cross-sections may be a consequence of the batch-to-batch differences induced at the factory. It is likely that these batch-to-batch effects will dominate the variations of cross-sections. Thus, it is very hard to estimate the systematic error of the measured SEU cross-sections.

The presented results confirm that devices made in technologies with smaller integration scales are more vulnerable to SEUs. Ref. [12] also contains cross-sections for neutrons.

In Ref. [14], the results of tests of dynamic SEUs in flip-flops are presented. The tests were performed similarly to our tests, i.e. the design containing long shift registers was tested. The authors observed the upset of flip-flops and determined a cross-section of $3.98 \times 10^{-14}\,\mathrm{cm}^2$ per flip-flop.

The main rival of Xilinx on the FPGA market is Altera. Unfortunately, Altera's FPGAs do not offer the read out of configuration bits. Therefore, the only way to measure the SEU susceptibility is indirect detection of configuration upsets through a VHDL design. Such tests are more complicated and their results less certain. Interesting results of ALTERA APEX EP20K400E tests performed in that way may be found in Ref. [16].

Confronting our FLASH memories results with other tests [7,10], it can be found that the most susceptible effects of total integrated dose (TID) element in such devices is a charge pump. The memory cell itself is resistant enough [10] and the SEUs during tests are results of SEUs in internal control logic [10].

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Irradiation Investigations for TESLA and X-FEL experiments at DESY

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ABSTRACT

Electronic components during High Energy Physics experiments are exposed to high level of radiation. Radiation environment causes many problems to electronic devices.

This report highlights the major hazards to electronics caused by radiation. Several experiments were done and results are included.

Keywords: Irradiation, gamma, neutron, TESLA, X-FEL, LINAC II, DESY, FPGA, TLD, LED, CCD, CMOS

1. INTRODUCTION

Two new projects TESLA (Tera Electon Volt Superconducting Linear Accelerator) and X-FEL (X-ray Free Electron Laser) are being developed at the DESY (Deutsches Elektronen-Synchrotron) in Hamburg, Germany. These projects are unique because of idea to place control electronic systems in collider tunnel, near superconducting cavities. It may cause many problems in routine work of electronic devices, because of its exposure to a moderate dose of neutron and gamma radiation.

The integrated flux of fast neutrons close to the cryomodule will be of the order of up to $1*10^{12}cm^{-2}/20$ years. The gamma dose rate close to the crymodule cannot exceed 10 rad / hour based on a maximum permitted additional cryo heatload of 0.1 W / m^2.

Main problems are due to ionization and displacement damage of semiconductors. This impact of the radiation on the electronic systems could appear as:

- single event upsets
- flipping bits in memory
- total ionizing dose effects
- reduction of life time of electronic components

In this case, there is a need of radiation sensivity investigations of electronic components. These tests should provide the information needed to optimize the design of electronics for TESLA and X-FEL and to minimalize failures during its operation.

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The irradiation experiments could be divided into three steps:

1. Radiation level measurements:
   - evaluation of radiation level in LINAC II and to compare with the radiation levels in TESLA and X-FEL
   - undestanding the radiation effects in superconducting linacs and measurements of radiation level in UV-FEL (neutrons, gamma radiation)
2. Investigation of radiation effects on electronic components and circuits - complete systems:
   - determine Single Event Effects (SEEs)
   - determine Total Ionizing Dose (TID) effects
   - determine radiation effects on different types of electronics
   - predict performance and life-time in TESLA and X-FEL tunnels
3. Counter measures:
   - develop radiation mitigation concepts and evaluate their performance in the presence of radiation

2. RADIATION EFFECTS ON ELECTRONICS

Radiation causes damages in electronic components. The type and magnitude of these damages depend on irradiation environment. There are three main groups of influence, depending on mechanism and caused effects: [3].

- Total Ionizig Dose (TID):
  Caused by neutrons, protons, heavy particles, gamma. It's degradation and/or failure as a function of ionizing radiation accumulation.
- Single Event Effects (SEE):
  Caused by neutrons. It's relatively instantaneous device upset or destruction (latchup, burnout, gate rupture).
- Displacement damages:
  Caused by heavy and secondary particles. It's the result from particles producing Non Ionizing Energy Loss (NIEL).

2.1. Total Ionizing Dose

Ionizing radiation causes electron-hole pairs creation in oxide (see Figure 1). Some of these pairs recombinate, more in the absence of electric field. All remaining electrons, because of their high mobility leave the oxide. Left holes, because of their very low mobility are mostly trapped. As the result there is positive charge trapped in the oxide.

2.2. Single Event Effects

Single highly ionizing particle (incident or secondary ion) penetrates through the oxide layer (see Figure 2). It provokes high electron-hole pairs density along its track and transient current across the oxide layer. In the result oxide breakdowns.

There can be different categories of Single Event Effects:

- Non-destructive results:
  - Single Event Upset (SEU) - bit flips in memory

  - Single Event Functional Interrupt (SEFI) - SEUs in device control logic (eg. in FPGA: JTAG TAP controller, Select Map interface)
  - Single Event Transient (SET) - changes in propagated signal

- Destructive results:
  - Single Event Gate Rupture (SEGR) - gate-to-channel short circuit
  - Single Event Burnout (SEB) - high instantaneous current $->$ junction breakdown
  - Single Event Latch-up (SEL) - Vdd-to-Vss short circuit

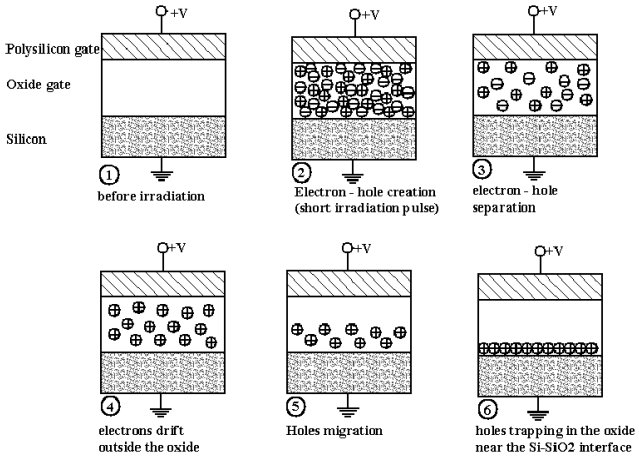

Figure 1. Cumulated ionisation example in MOS oxide [3]

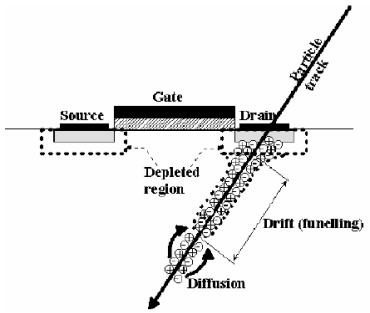

Figure 2. Example of Single Event Effect - Single Event Upset [3]

2.3. Displacement Damage

Heavy or secondary particle collides with atoms from crystal structure of the semiconductor material. It causes defects in this structure along the track of particle.

The effects of displacement damage could be:

- minority carrier's lifetime decreases
- carrier's mobility decreases
- effective majority carrier's concentration decreases - resistivity increases
- creation of acceptor levels - type inversion (N $->$ P)

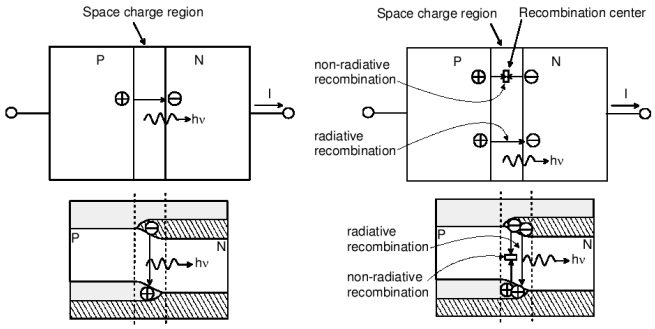

Figure 3. Creation of recombination center in P-N junction caused by displacement damage [3]

3. IRRADIATION TESTS OF ELECTRONIC COMPONENTS

Because of inaccessibility of TTF-II tunnel, these experiments were carried out in Linac 2 tunnel. The test system and linac itself is described below. It should be mentioned that future tests are planned to be prepared in UV-FEL tunnel.

Some electronic components have been tested:

- Thermo Luminescent Dosimeters (TLD)
- Light Emitting Diodes (LED)
- Charge-Coupled Device (CCD) Cameras
- Field Programmable Gate Array chips (FPGA)

All experiments and the results are presented below.

3.1. Linac 2 test system

Linac 2 is DESY's only electron accelerator injecting high energy electrons (450 MeV) to booster synchrotron DESY 2. It consists of two parts (see Figure 4). First one accelerates electrons produced by 150 keV electron source. Electrons with energy about 450 MeV hit the tungsten conversion target and produce electron-positron pairs. There are also neutrons and gamma radiation produced as a parrasitic radiation. The positrons are stored in Positron Intensity Accumulator (PIA), and then delivered to DESY 2, booster synchrotron. [1]

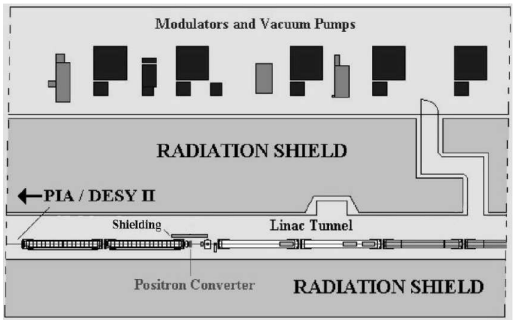

Figure 4. Linac 2 tunnel

The radiation environment in Linac 2 tunnel is not well known. The only value which can help quantify it is PIA current. This current coresponds to number of electrons hitting the converter and to parasitic radiation. The accumulated PIA current (PIA charge) corresponds to total neutron and gamma dose.

During the experiments Devices Under Tests (DUT) were placed in various positions along the tunnel (see Figure 4). Changing the distance between the DUT and e^-/e^+ converter allows to change radiation level. Its lowest value is near the entry corridor, about 20 meters from the target and the highest near the converter. It should be pointed that electron-positron converter is placed behind the lead shield. This shielding reduces radiation intensity.

3.2. Thermo Luminescent Dosimeter irradiation experiments

3.2.1. Introduction

Thermo Luminescent Dosimeter is made of Lithium Fluoride. After exposure, the device is heated to 400 Celssius degrees. This causes them to emit luminescence signal, whereas iths intensity is proportional to radiation exposure. Glow curves of the readout show accummulated radiation dose.

Thermo Luminescent Dosimeter 100 (TLD-100) is mainly sensitive to gamma radiation.

3.2.2. Experiment and results

TLD 100 samples were placed in different positions along the tunnel for 23 hours. The results are shown in the Table 1.

Integrated PIA current during 23 hours of experiment was 76.626 mA.

Table 1. TLD results

Distance from converter [m]	0	0.5	1	2	4	8	12	16
Dose [Sv]	102.3	117.9	113.0	149.0	32.5	4.9	1.9	1.2

The experiment provides information about irradiation doses along the Linac II tunnel. The doses depend on position of DUT in the accelerator tunnel. The influence of lead shielding is also evident. TLDs placed near the converter (distances: 0, 0.5, 1 meter) but behind the curtain show lower accumulated dose than TLDs placed at 2 meter.

3.3. Light Emitting Diodes irradiation experiments

3.3.1. Introduction

It's known that neutron flux causes the displacement damage of p-n junction in semiconductors, such as Light Emitting Diodes (LED). Light emitting diodes (LED) suffer irreversible damage after irradiation with fast neutrons. The LEDs exposed to neutrons produce less luminescence light than unexposed (control) LEDs, connected to a constant current source.

3.3.2. Experiment

The proposed experiment aims to investigate the radiation damage phenomena of the LED irradiated with accelerator produced neutrons. The chosen LEDs are yellow 3 mm light emitting diodes from Panasonic (LN48YPX). The plan of the experiment is summarized below:

1. Estimation of the light output characteristics of a group of yellow LEDs operated at various input current level.
2. Irradiation of the LEDs with fast neutrons in the available accelerator tunnel at various exposure (dose) levels.
3. Evaluation of the LEDs.
4. Data analysis and estimation of the neutron flux.

Simple instruments including a photometer, constant current power supply, digital multimeter and a custom designed aluminum cup was used in this test (see Figure 5).

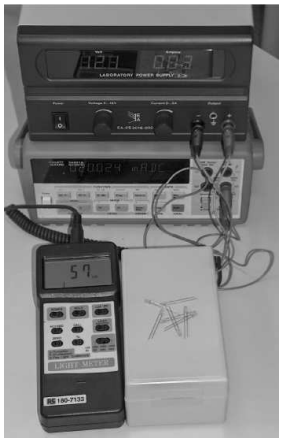

Figure 5. LEDs test system, consisting of light meter (RS V10860), multimeter (HP 34401A) and power supply (EA-PS 2016-050).

Results for unirradiated LEDs operating various input currents (control reading) shows Figure 6. There were made several irradiation runs. The results - relationship between LEDs relative light attenuation and PIA accumulated current shows Figure 7.

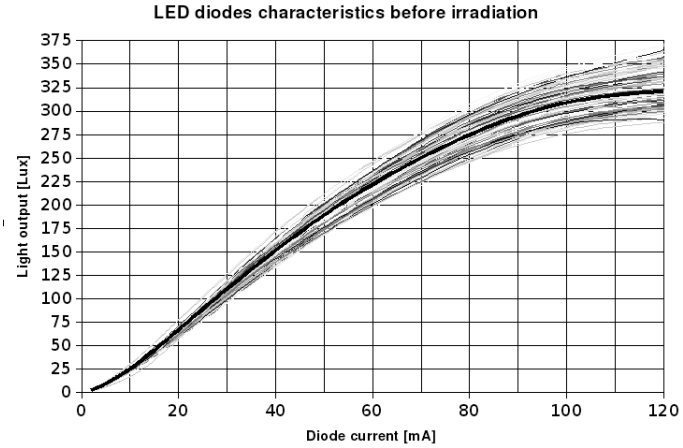

Figure 6. LEDs control reading, black bold line shows avarage value

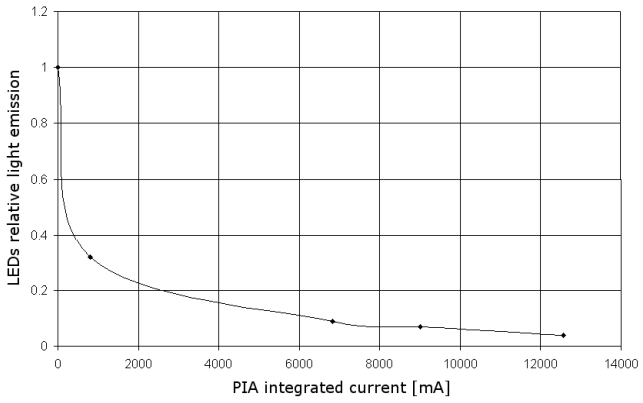

Figure 7. LEDs relative light emission as a function of PIA accumulated current, LEDs were evaluated with a forward current of 20 mA

The Figure 7 proves that irradiation destroys p-n junction in light emitting diodes. The light output becomes smaller proportionally to PIA integrated current and to accumulated radiation doses.

3.4. CCD sensors irradiation experiments

3.4.1. Introduction

The goal of the experiment was to use Charge Coupled Devices (CCD) sensors as radiation detector. Find dependence between radiation hardness of CCD and total integrated dose and radiation level, also estimate the device lifetime.

CCD was chosen because it is much more sensitive to radiation damage than other types of semiconductor elements. Signal charge packets travel over a much longer path before being registered, and the readout method (moving signal row by row from the image area into the output register, with a subsequent shift in the output register to the output node) increases the time a signal is subject to loss.

Tests took place in Linac II tunnel in DESY Hamburg and show that radiation influence causes two defects: dark current increase and increase of number of hot pixels. Measurements were calibrated with LED diodes tests.

3.4.2. Tests and theory

We tested commercially available CCD and build a model for the radiation damage effects. Structure of a CCD sensor is schematically shown on Figure 8. The epitaxial layer of $\sim 20\mu m$ thick is the sensitive region.

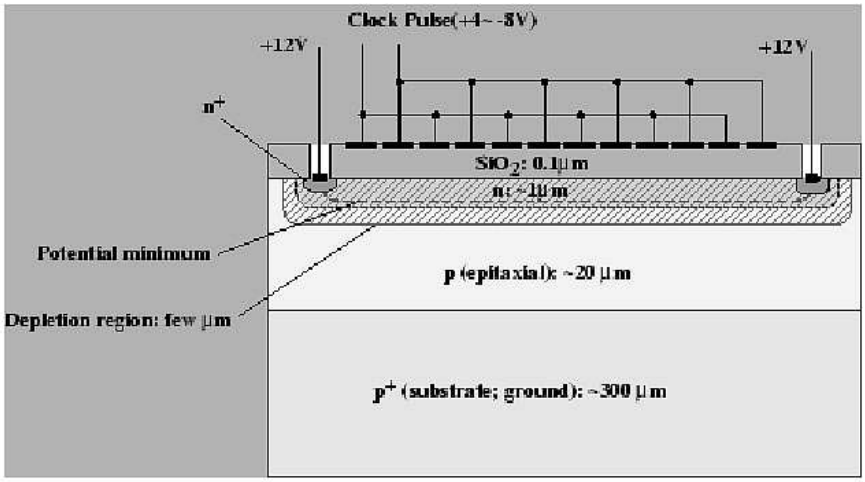

Figure 8. Structure of a CCD sensor [7].

Because of the type and the energy spectrum of the radiation, surface and bulk damage effects happen in the CCD sensors. Ionizing radiation creates electron-hole pairs in silicon dioxide, which is used as gate and field dielectric in CCDs. Charge carriers drift in the electric field (externally applied or built-in) to the corresponding electrode. Electrons quickly reach the positive electrode, but some of the holes remain trapped in the oxide and give rise to radiation-induced trapped positive oxide charge, which can be stable for long time. This **surface damage** is dominant source of dark current in CCDs.

High energy radiation can displace Si atoms from their lattice positions, creating displacement damage (**bulk damage**). Low energy electrons and X-rays can deliver only small energy to the Si atom and isolated displacements, or point defects, can be created. But heavier particles, like protons and neutrons can knock out

silicon atoms which can displace other atoms in the crystal. This bulk defects also cause dark current to increase. Irradiation with heavy particles (e.g. protons, neutrons) creates "dark current spikes", also known as "hot pixels" – pixels with much higher dark current than the average value for the CCD (see Figure 9 and Figure 10). Their presence is connected with the high electric fields caused by the device architecture and field-enhanced emission, the cluster nature of the radiation damage and crystal strains in the silicon material [7].

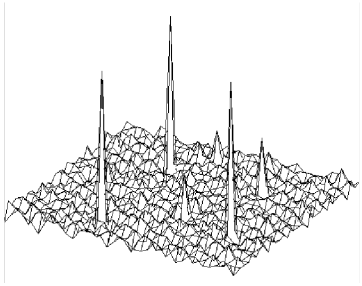

Figure 9. Hot pixels 3D.

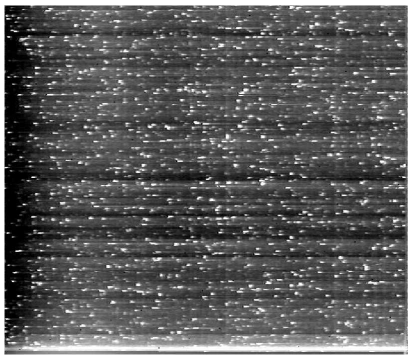

Figure 10. Hot pixels image.

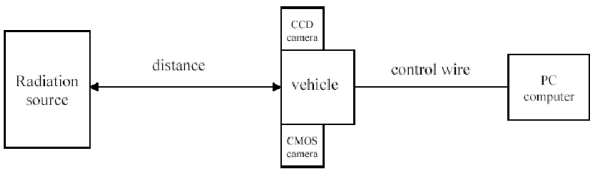

Figure 11. Test system.

3.4.3. Test system

The test system was build with CCD and CMOS cameras connected to PC with coaxial cable (see Figure 11). Images were taken and processed by PC, radiation level controlled by changing distance to radiation source. The system was remote controlled by TCP/IP network.

Online monitoring software was based on Linux operating system, language C/C++ and TCL/TK, Perl scripts. It used **bttv** module image grabber (**V4L** interface). Algorithm consisted in grabbing image, count and store number of hot pixels:

- grab image (**V4L** interface, **bttv** module image grabber),
- find and count hot pixels (see Figure 9 and 10)
  - multiply image by upper transmit filter (to reduce background) and find local maxims,
  - count hot pixels,
- store the number of hot pixels in database (save selected images),
- switch on, switch off cameras power supply to check if hot pixels are permanent defects,
- finally calculate data in and draw diagrams in **octave**.

3.4.4. Experiment and results

- **Number of hot pixels during the experiment**

  One of effects happened by irradiation CCD sensors are hot pixels. To check what dependence is between number of hot pixels and total integrated dose we draw number of hot pixels and integral of PIA current on one Figure 12 and 13. Number of hot pixels rises when there is PIA current – integral of PIA current rise (see Figure 12).

  To check nature of hot pixels we switch on and switch off power supply of CCD sensors (0 hot pixels - camera switched off, Figure 12). The number of hot pixels quickly increases after switch on and stops on permanent level (see Figure 13). This is example of theoretically predicted **bulk damage** and shows that hot pixels are permanent effects.

- **Image histogram, "dark current" during the experiment**

  Other effect happened during irradiation of the CCD sensor is the "dark current" increase. During the experiment we observe that "dark current" increase, maximum of the shape of histogram moves to left and staying wider (see Figure 14 and Figure 15). It confirms theoretically predicted **surface damage**.

- **Number of hot pixels in function of total integrated dose**

  To use CCD sensor as radiation sensor we need to estimate number of hot pixels in function of total integrated dose. We count deltas of number of hot pixels, and then count integral and draw diagram in function of integral PIA current (see Figure 16).

  It seems to be a linear dependence, hence approximated with a first degree polynomial (see Figure 16).

  $$pix = 0.000119 \cdot pia + 0.0332$$

  where: pix - integral deltas of number of hot pixels [percents], pia - integral PIA current

  Calibration with LED diodes shows total integrated dose was:

  $$1.81 \cdot 10^{11} \frac{neutrons}{cm^2}$$

  We can count that dose $0.4 \cdot 10^{11} \frac{neutrons}{cm^2}$ cause increase 0.1 percent of hot pixels.

The measurements show that neutron irradiation of CCD-s with a dose of $2 \cdot 10^{11} \frac{neutrons}{cm^2}$ creates noticeable effects on the CCD. The increase of number of hot pixels can be approximated as linear function of integrated dose. It allows use CCD sensors as low-cost radiation detector.

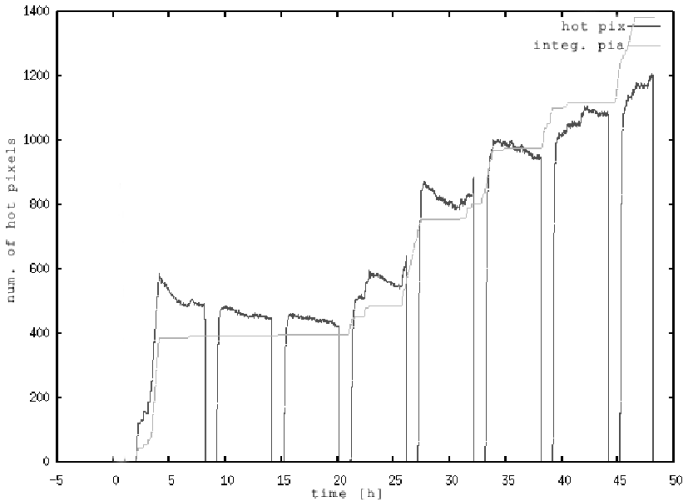

Figure 12. Number of hot pixels on CCD camera and integral of PIA current.

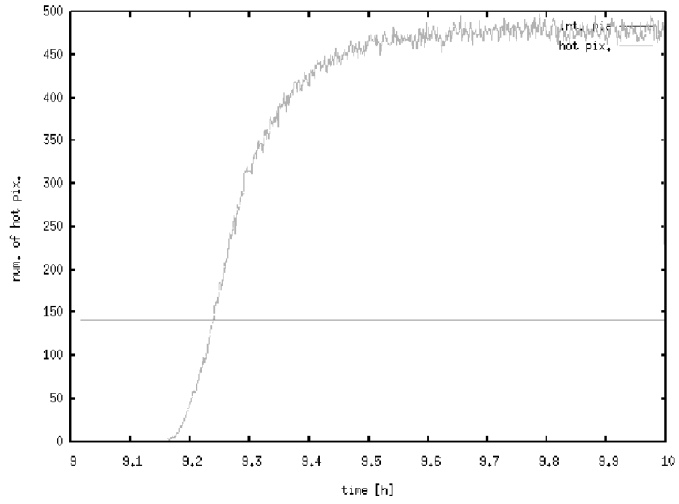

Figure 13. Number of hot pixels on CCD camera after "power on", no PIA current.

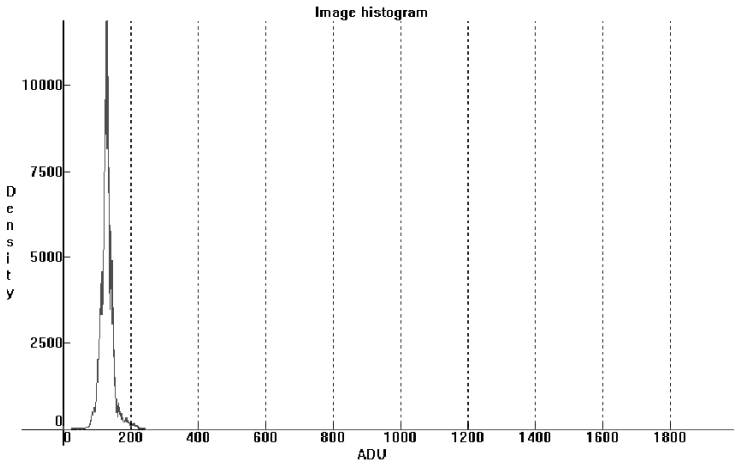

Figure 14. Histogram of CCD signal output after 3.5 hours.

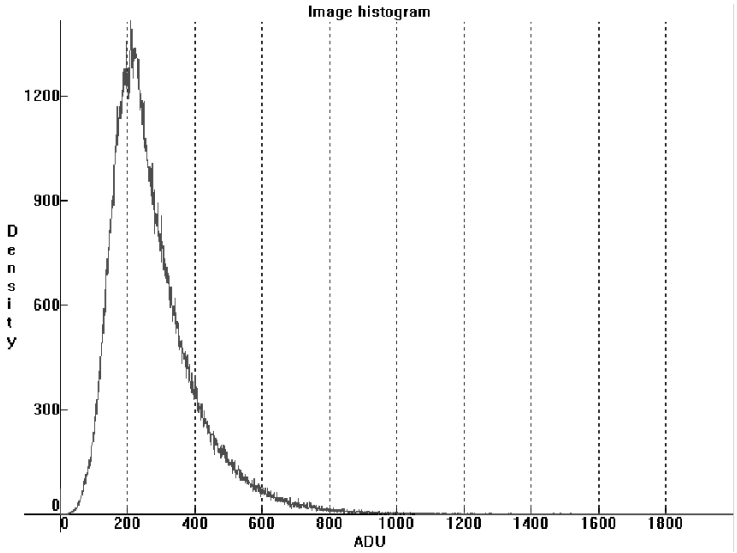

Figure 15. Histogram of CCD signal output after 9 days.

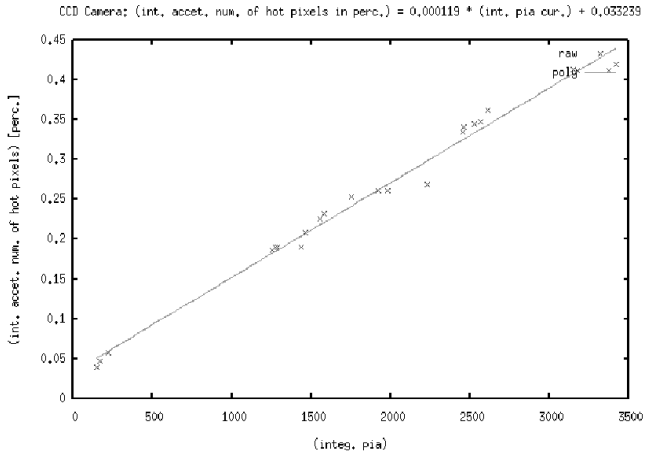

Figure 16. Integral deltas of number of hot pixels as a function of integral PIA current.

3.5. Field Programmable Gate Arrays irradiation experiments

3.5.1. Field Programmable Gate Array technology

Field Programmable Gate Array chips (FPGAs) are type of programmable circuits, which are programmed by user to perform the designed functionallity. Project must be written in one of Hardware Description Language (HDL), e.g. VHDL, Verilog. It's compiled, synthesized and implemented in FPGA chip. The configuration bits can be stored in a chip using different techniques depending on technology:

- Antifuse technology - programmable only once,
- Flash memory - programmable several times,
- SRAM memory - programmable dynamically.

The last possibility is dominating technology. It allows very fast, almost unlimited in system reprogramming.

Architecture of FPGA chips from different vendors may differ but the main idea is almost the same. It consists of some main blocks (description based on Xilinx Spartan-IIE chip, see Figure 17):

- Flexible, programmable Configurable Logic Blocks (CLB), which provide the functional elements for constructing logic. The basic block of the CLB is Logic Cell (LC). Two LCs form slice and two slices form CLB. Each LC includes a function generator, carry logic and a storage element. The function generator is implemented as look-up table (LUT). The storage element can be configured either as edge-triggered D-type flip-flop or as level-sensitive latch.
- Programmable Input/Output Blocks (IOB), which provide the interface between the package pins and the internal logic. The IOB features inputs and outputs that support a wide variety of I/O signalling standards. Each input and output can be configured to conform to any of the low-voltage signalling standards.

- Delay-Locked Loops (DLL) for clock distribution. This block eliminates skew between the clock input pad and internal clock-input pins throughout the device. Additionaly delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input.
- Dedicated internal memory (Block RAM). That's internal memory that can be used to storage data inside the chip. The word length and type of memeory can be configured by system designer.
- Versatile multi-level interconnection structure. Local routing resources provide three types of connections:
  - interconnections among the LUTs, flip-flops,
  - internal CLB feedback paths, between LUTs in the same CLB,
  - direct paths providing high-speed connections between horizontally adjecent CLBs.

  The software automatically uses the best available routing based on user timing requirements.

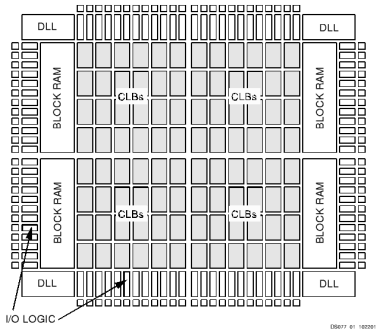

Figure 17. Basic Spartan-IIE Family FPGA Block Diagram [9]

Values stored in static memory cells control all the configurable logic elements and interconnection resources. These values must be loaded into the memory cells on power-up and can be reloaded to change function of the device, almost any time.

3.5.2. Radiation induceed errors in FPGA chips

The two most important components of a FPGA chip where radiation failures occur are SRAM (Static Random Access Memory) cells and flip-flops. The most probable errors are related to Single Event Effects, particularly Single Event Upsets.

Single Event Upset (SEU) is a change of a logic state of an element storing one bit caused by radiation. Two types of SEUs may be distinguished:

- static SEUs - changes in the configuration bits
- dynamic (or transient) SEUs - changes the logic state of the bits, which are supposed to change during normal operation (for example flip-flops)

SEUs affect the performance of FPGA in different ways. Changing the state of one flip-flop working as a latch results in false value of one bit during one clock period only, while changing the state of one SRAM cell in look-up table results in a permanent wrong answer for one combination of input bits. Changing the state of one SRAM that programs the interconnection between logic blocks can seriously modify the performance of whole circuit. [4]

3.5.3. Test board and system

For the irradiation experiments the SRAM-based FPGA chip from Xilinx company - Xilinx XC2V1000 was used. Chip was mounted on Virtex-II LC 1000 Memec Development Kit (see Figure 18). This board also utilizes:

- serial interface (RS-232 C)
- voltage regulators
- DDR and PROM memories
- oscillators
- LED display

Figure 18. Virtex-II LC 1000 Memec Development Kit [°]

The test board was connected with computer placed outside the irradiated area. Connection provides configuring and verifying of FPGA chip by JTAG interface. There was appropriate software running on computer, performing test routine (see Figure 19) automatically.

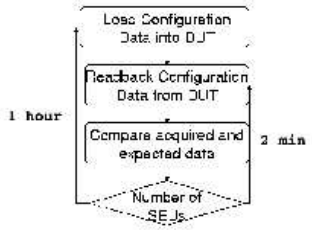

Figure 19. FPGA test routine

Test routine (see Figure 19) allows to verify FPGA configuration memory. Programming DUT with dummy project was performed every 1 hour. The reading back configuration was done every 2 minutes. The result was compared with bitstream with which DUT was programmed. The number of different bits shows number of static errors in configuration memory of FPGA.

3.5.4. Results of the experiment

The results of tests are shown in Figure 20. Picture presents total number of SEUs in configuration memory and integrated PIA current during each day of experiment. There is strong relationship between these values.

On the other hand there were only SEUs observed, no permanent destruction of FPGA chip. Also there were no problems with voltage regulators and JTAG interface. These elements worked correctly.

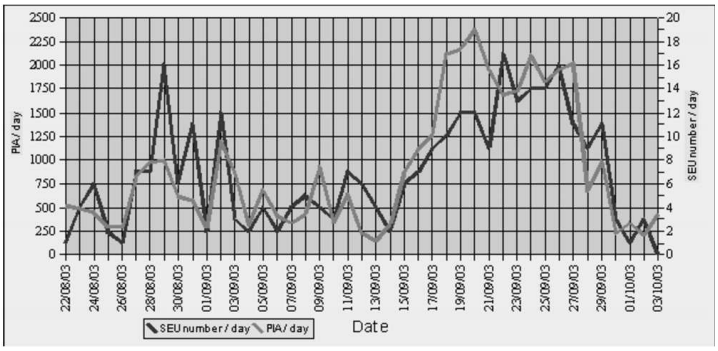

Figure 20. SEUs in FPGA configuration memory

4. COUNTER MEASURES METHODS

Irradiation experiments show that special methods of mitigation of radiation effects are needed. There are several ways to perform it:

- Conventional shieldings
- Chips dedicated to work in irradiation environment
- Appropriate system design (eg. Triple Module Redundancy)

4.1. Conventional shieldings

Estimated maximum value of gamma radiation is about 10 rad / h = about 10^6 rad / 20 years. The maximum Total Ionizing Dose for electronic devices is about a few krads. In this case gamma field should be reduced to 0.1 % to secure in-tunnel electronics. The best substance for this purpose is concrete. This material has HVL factor about 100 mm, for gamma radiation energy 5 MeV. Half-Value Layer (HVL) is the thickness of material to reduce gamma radiation to half [6]. To reduce gamma to 0.1 % there should be used $10 * 100mm = 1m$ of concrete wall.

Neutrons for electronic devices is not a critical problem. They cause only not-permanent errors [4]. Shielding againt neutron radiation is less important.

4.2. Dedicated electronics for radiation environment

Some companies produce chips designed to work in high radiation environment. For example it could be XQR family of Xilinx FPGA chips. It has bigger (200 krads instead of tens krad) Total Ionizing Dose. This chips have longer lifetime exposed to high radiation.

There are also whole electronic systems dedicated to radiation environment. Maxwell company produces SCS750 board wich includes 3 PowerPC on it. In comparison to commercial PowerPC it can withstand a dose in excess of 100 krad. It has also incredible high SEU rate ($< 9 * 10^{-6}$ upset per day on GEO orbit).

The main disadvantage of such rad-hard devices is high cost. It is many times higher than price of normal, commercial devices.

4.3. Appropriate system design

There are some methods to mitigate irradiation problems with electronic devices by designing appropriate system schematic. For example it could be (in the brackets there is name of the effect against which method protects):

- Current Limiting (SEL, SEB)
- Software and hardware error detection and correction (SEU)
- Constant refreshing (SEU)
- Redundancy triple voting - TMR (SEU):

These ideas are presented in other publications, eg. [3].

5. CONCLUSIONS

All experiments show that irradiation of electronic devices causes damages. Depending on that information there is a possibility of buidling systems to measure radiation using Light Emitting Diodes and Charge Coupled Devices as radiation detectors. Although control and calibration experiments should be performed.

Next point is that errors in Field Programmable Gate Arary chips are Single Event Upsets. There are caused mainly by neutrons. Gamma radiation only limits lifetime of devices but does not causes improper work.

The results of experiments show some radiation mitigation methods should be used to ensure electronic system will work properly in the tunnel. Previous chapter of this article presented several new concepts. We are planning to conduct thorough experiments in order to investigate the function of complex electronic systems in various radiation environments of interest. A suitable counter measures could be selected from the above experimental results.

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D. Rybka, A. Kalicki, K. Poźniak, R. Romaniuk, B. Mukherjee, S. Simrock, ***Investigations of Irradiation Effects on Electronic Components to be used in VUV-FEL and X-Fel Facilities at DESY,*** **Proceedings of SPIE, Volume 5948 (being published)**

Investigations of Irradiation Effects on Electronic Components to be used in VUV-FEL and X-FEL Facilities at DESY

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ABSTRACT

Electronic components during High Energy Physics experiments are exposed to high level of radiation. Radiation environment causes many problems to electronic devices.

The goal of several experiments done at DESY (Deutsches Elektronen Synchrotron, Hamburg) was to investigate nature of irradiation effects, caused damages and possible techniques of mitigation.

One of aspects of experiments is radiation measurements. The propositions of building radiation monitoring system, using different semiconductor components, are presented.

Second aspect is radiation tolerance. Different electronic devices were tested: FPGA chips, CCD sensors, bubble dosimeters and LED diodes. Components were irradiated in TESLA Test Facility 2 tunnel and in laboratory using $^{241}Am/Be$ neutron source. The results of experiments are included and discussed.

Keywords: Radiation, gamma, neutron, $^{241}Am/Be$, VUV-FEL, X-FEL, TESLA, DESY, FPGA, LED, CCD, bubble dosimetry

1. INTRODUCTION

The X-Ray Free Electron Laser (X-FEL) is being developed at the Deutsches Elektronen Synchrotron (DESY) in Hamburg, Germany. This facility will be built using niobium superconducting cavities (TESLA technology), producing moderate dose of neutron and gamma radiation during operation. As some electronic systems for controlling X-FEL will be placed in the accelerator tunnel, the radiation tolerance of the electronic devices should be measured.

Radiation studies for X-FEL are divided into three steps[1]:

1. Radiation measurements:
   - understanding the radiation effects in superconducting linacs,
   - measurements of radiation level in VUV-FEL,
   - development of new radiation measurements techniques.
2. Investigations of radiation effects on electronic components and circuits.
   - determine Single Event Effects (SEE), Total Ionizing Dose (TID), Displacement Damages,
   - comparing different types of electronics,
   - predict performance and life-time in X-FEL tunnel.
3. Development of electronic system for X-FEL working in radiated environment.

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2. RADIATION EFFECTS ON ELECTRONIC COMPONENTS

Radiation produces different effects in electronic components. There are three groups of influence, depending on mechanism and caused effects[1,9]:

- Total Ionizing Dose (TID) - degradation and/or failure as a function of ionizing radiation accumulation. Ionizing radiation creates electron-hole pairs in oxide. Some of these pairs recombinate, escpecially in the absence of electric field. All remaining electrons, because of high mobility leave the oxide. Holes, because of low mobility, are mostly trapped. As the result there is positive charge trapped in the oxide.

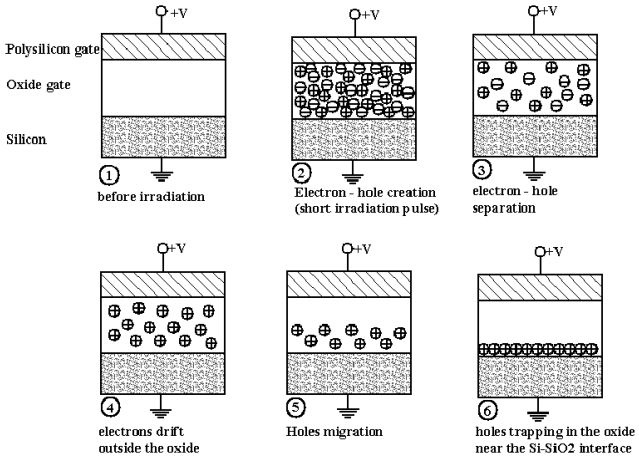

Figure 1. Cumulated ionisation example in MOS oxide[9]

- Single Event Effects (SEE) - relatively instantaneous device upset or destruction (latchup, burnout, gate rupture). Single highly ionizing particle (incident or secondary ion) penetrates through the oxide layer. It provokes high density of electron-hole pairs creation along its track and transient current across the oxide layer. As the result the oxide breakdowns. There are different categories of Single Event Effects:
  - with non-destruction results:
    - Single Event Upset (SEU) - flipping bit in memory,
    - Single Event Functional Interrupt (SEFI) - SEU in device control logic (eg. JTAG TAP controler, Select Map interface,
    - Single Event Transient (SET) - changes in propagated signal.
  - with destructive results:
    - Single Event Gate Rupture (SEGR) - gate-to-channel short circuit,
    - Single Event Burnout (SEB) - high instantaneous current → junction breakdown,
    - Single Event Latch-up (SEL) - Vdd-to-Vss short circuit.

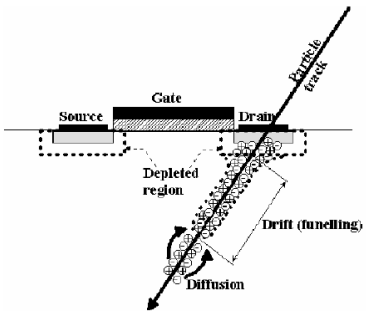

Figure 2. Example of Single Event Effect - Single Event Upset[9]

- Displacement damages - the result from particles producing Non Ionizing Energy Loss (NIEL). Heavy or secondary particle collides with atoms from crystal structure of the semiconductor material. It causes defects along the track of the particle. It can effects in:
  - minority carrier's lifetime decreases,
  - carrier's mobility decreases,
  - effective majority carrier's concentration decreases - resistivity increases,
  - creation of acceptor levels - type inversion (N → P).

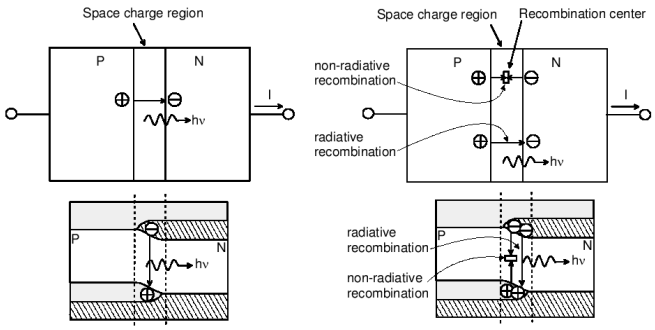

Figure 3. Creation of recombination center in P-N junction caused by displacement damage[9]

3. RADIATION FACILITIES

Experiments described below took place in two radiation environments:

- in TESLA Test Facility II tunnel,
- in laboratory using $^{241}Ab/Be$ neutron source.

3.1. Tunnel of TESLA Test Facility II

TESLA Test Facility II (TTF2) is a test system for ILC (International Linear Collider) and VUV-FEL and X-FEL experiments at DESY, based on TESLA technology. The same technology will be used in future accelerators.

The DUTs (Devices Under Tests) were placed in different locations inside the tunnel (see Figure 4) to vary the radiation levels. The experiments were done using unmeasured parasistic radiation from accelerator.

Figure 4. TESLA Test Facility II tunnel

3.2. $^{241}Am/Be$ neutron source

For the experiments there were used simple neutron irradiation facility with variable avarage energy using a light water moderated $^{241}Am/Be$ source (see Figure 5).[5] The neutron spectrum of this setup is to be very similar to neutron field generated from electrons with energy about 1.6 GeV on niobium material. Niobium is used for manufacturing cavities in VUV-FEL and X-FEL experiment.

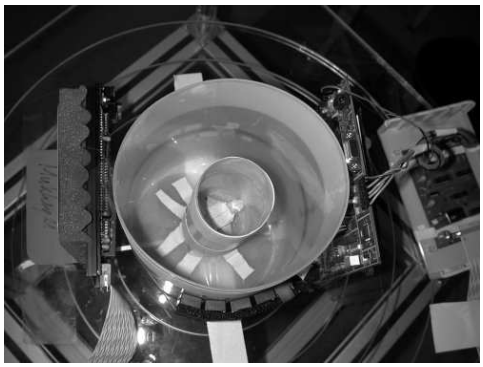

Figure 5. Plastic jar for $^{241}Am/Be$ neutron source and light water moderator

Using light water moderation the average neutron energy decreases from 5.1 MeV to 3.3 MeV (for a moderator thickness of 6.5 cm). Maximum of neutron flux moves to lower energy.[5]

4. AUTOMATIC DOSE READER FOR NEUTRON BUBBLE DETECTORS

4.1. Neutron bubble detector

The detector consists of an elastic polymer with droplets of superheated liquid. When neutrons got stuck in these droplets, they form small gas bubbles. The bubbles remain fixed in the polymer to provide a real time record of the dose (see Figure 6).

Bubble dosimeter is reusable, the number of bubbles formed is directly proportional to the dose. Response is independent of dose rate. Detectors are very compact and light-weight. Bubble dosimeters are produced by BTI (Bubble Technology Industries).

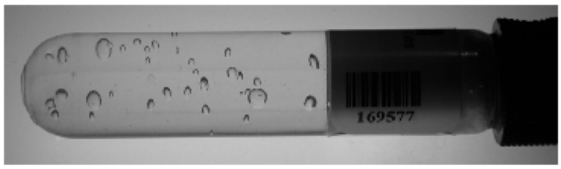

Figure 6. Neutron bubble detector

4.2. OBCA - Optical Bubble Counting Algorithm

Optical Bubble Counting Algorithm (OBCA) is developed for automatic reading of bubble dosimeters.[8,7] It consists of four functional parts:

- reading of the image,
- detecting edges with Canny edge detection filter,
- eliminating straight lines and small objects,
- counting bubbles.

The software is written in JAVA Swing, it can read any type of image file (jpg, bmp, etc.) and runs on any operating system with JRE (Java Runtime Environment). Figures 7 – 9 show user interface during operational steps of algorithm: image reading (see Figure 7), edge detection (see Figure 8) and bubbles counting (see Figure 9). During every processing stage the image can be saved as bitmap file (bmp).

4.3. Results

The bubble dosimeters were irradiated with neutrons and then evaluated. Number of bubbles manually counted by three different persons and counted by OBCA v. 1 are presented in Table 1.

Table 1. Number of bubbles manually counted by three different persons and counted by OBCA v. 1

Method/Angle	0/360 °	90 °	180 °	270 °	Average	Diff. (%)
Manual 1	227	220	217	245	227.45	4.5
Manual 2	227	232	247	293	249.75	-4.9
Manual 3	209	242	260	249	240	-0.8
OBCA v 1	252	223	227	239	235.25	1.2

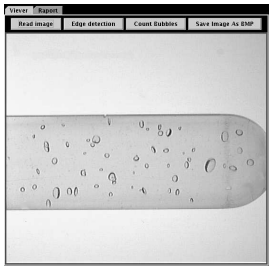

Figure 7. OBCA, 1st step - image reading

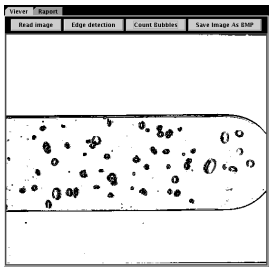

Figure 8. OBCA, 2nd step - edges detecting

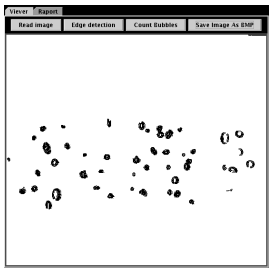

Figure 9. OBCA, 3rd step - bubbles counting

4.4. Conclusions

The algorithm works correctly. As shown in the Table 1, error number of counted bubbles is small (even for manual counting is few percents). A problem with elimination of non bubble objects causes algorithm accuracy decrease. Especially when there are overlapped bubbles. The algorithm can be used for real-time bubble monitoring.

5. DIGITAL PHOTOMETER FOR COTS LED FAST NEUTRON DOSIMETER

5.1. Introduction

It's known that neutron flux causes the displacement damage of p-n junction in semiconductors, such as Light Emitting Diodes (LED). Light emitting diodes (LED) suffer irreversible damage after irradiation with fast neutrons. The LEDs exposed to neutrons produce less luminescence light than unexposed (control) LEDs, connected to a constant current source.[6]

5.2. Device

There were built dedicated photometer for Commercial-Off-The-Shelf (COTS) Light Emmiting Diodes fast neutron dosimeter (see Figure 10).[1,2]

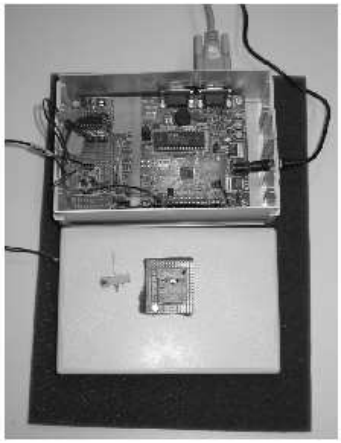

Figure 10. Digital photometer for COTS LED fast neutron dosimeter

There were also developed software in Python language to perform measurements and taking data from device (see Figure 11).

Figure 11. Control panel of application for LED light output measurements

Preliminary investigations proved the device and method are working correctly.[2]

6. INVESTIGATIONS OF SEUS AND PERMANENT DAMAGE IN COTS CCD CAMERAS

The theoretical aspects of CCD (Charge Coupled Device) cameras radiation damage and automatic recognition algorithm are described in other publication.[1]

6.1. Plan of experiment

There were tested popular Commercial-Off-The-Shelf CCD-Camera-Modules available in Conrad shop (Best.-Nr. 11 67 50) with sensor size: 500 [H] x 582 [V] pixels (291000 pixels).

Figure 12 shows the test system. As a neutron source there were used $^{241}Am/Be$. Cameras were put in different distances from the source: 6.5 cm and 13 cm. Water moderator thickness was 0, 6.5 and 13 cm. There were made also tests with and without Cd (Cadmium) shielding. Cameras where connected to PC with frame-grabber. Each second PC got image, processed and counted white pixels (camera's sensor was shielded to get black image).

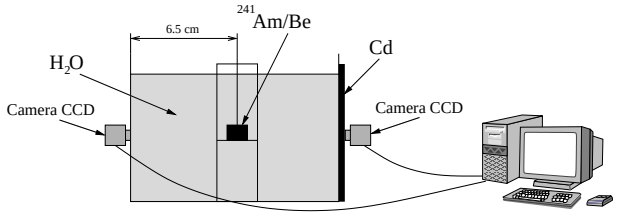

Figure 12. CCD cameras radiation experiments test system

6.2. Results

The results are presented in Table 2 and on Figures 13 – 15. Figures show number of permanent and single event defects as a function of time. Numbers where averaged by 10 (10 seconds).

Table 2. CCD cameras radiation experiments results

Fig.	dist. cm	H_2O cm	Cd	source min.	dos. min.	dos. nr	bub.	$\mu Sv/b$	μSv	per.	SEU
13	6.5	-	-	30	-	-	-	-	-	12	7
14	6.5	6.5	-	20	10	169602	35	7.8	273	2	6
15	6.5	6.5	+	30	10	169577	42	7.2	302.4	3	0.5
-	13	13	-	10	10	169774	15	7.2	108	0	1.5
-	13	6.5	+	10	10	170070	17	8.4	142.8	0	0.4
-	13	6.5	-	10	10	170377	16	6.1	97.6	0	2

6.3. Conclusions

Water moderation reduced number of permanent defects on CCD sensor from 12 to 2 (see Figures 13 and 14). It means permanent defects on CCD sensors are caused by fast neutrons.

SEU in CCD sensors are caused by thermal neutrons (low energy), which can be stopped by Cd shielding (see Figure 15).

In other experiments distance from neutron source to CCD camera (13 cm) was too big to observe noticeable damage effects on CCD sensor.

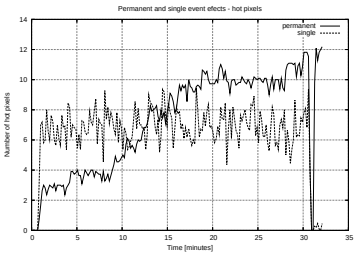

Figure 13. CCD cameras radiation experiment results (distance 6.5 cm, no water, no Cd, no bubble dosimeter, source in for 30 min.)

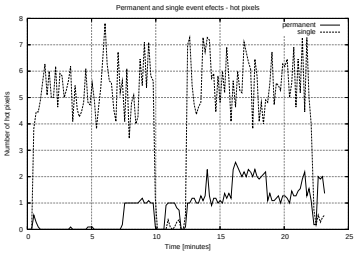

Figure 14. CCD cameras radiation experiment results (distance 6.5 cm, water 6.5 cm, no Cd, bubble dosimeter reading: 35 bubbles - dose 273 μSv (for 10 min.), source in for 20 min.)

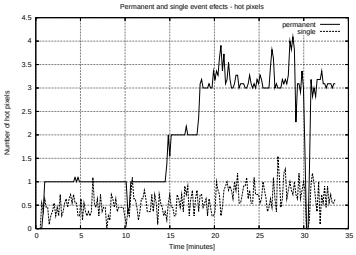

Figure 15. CCD cameras radiation experiment results (distance 6.5 cm, water 6.5 cm, with Cd, bubble dosimeter reading: 42 bubbles - dose 302.4 μSv (for 10 min.), source in for 30 min.)

7. INVESTIGATIONS OF STATIC SEUS IN FPGA CHIPS

7.1. Radiation induceed errors in FPGA chips

The two most important components of a FPGA chip where radiation failures occur are SRAM (Static Random Access Memory) cells and flip-flops. The most probable errors are related to Single Event Effects, particularly Single Event Upsets.

Single Event Upset (SEU) is a change of a logic state of an element storing one bit caused by radiation. Two types of SEUs may be distinguished[4]:

- static SEUs - changes in the configuration bits
- dynamic (or transient) SEUs - changes the logic state of the bits, which are supposed to change during normal operation (for example flip-flops)

7.2. Test system

Developed test system for FPGA static and dynamic SEU (see Figure 16) consists of:

- DUT (Device Under Test) - FPGA board,
- Personal Computer,
- Converter boards - providing long connections using RS 485 protocol,
- Power supply.

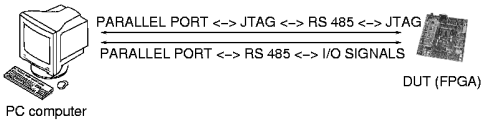

Figure 16. Test system for FPGA radiation experiments

There were developed dedicated software in Python language. Control panel is presented on Figure 17. It allows to perform investigations of static and dynamic SEUs paralelly or separately.

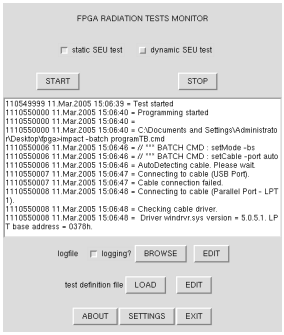

Figure 17. Control panel of application for FPGA radiation tests

7.3. Experimental results - TESLA Test Facility 2

There were performed only radiation experiments of configuration memory (static SEUs) of FPGA. The DUT was placed just after first accelerating module, about 2 meters from accelerator tube, near the wall. Test was performed for 42 days of operational work of TTF2 accelerator. FPGA was programmed every day.

The results (number of Single Event Upsets per day and time before Single Event Upset) are presented on Figure 18 and 19.

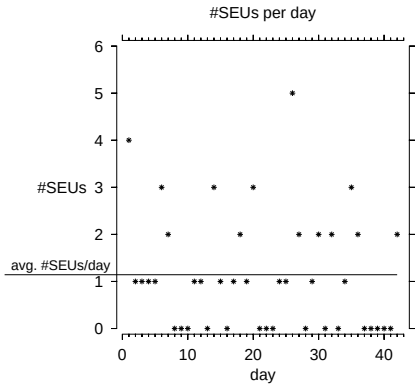

Figure 18. Results of FPGA radiation experiments in TESLA Test Facility 2 tunnel - Single Event Upsets per day

The avarage number of Single Event Upsets per day during the whole experiment was about 1 (see Figure 18). It proves that FPGA could work in such environment without big problems because of SEUs.

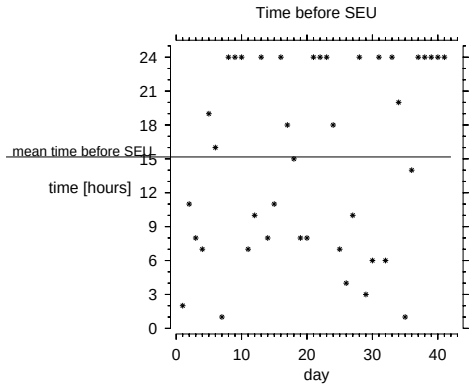

Figure 19. Results of FPGA radiation experiments in TESLA Test Facility 2 tunnel - Time before Single Event Upset

The mean time from programming FPGA to first Single Event Upset during the whole experiment was about 15 hours (see Figure 19). It proves that often refreshing of the FPGA configuration memory prevents it from uncorrect work.

7.4. Experimental results - $^{241}Am/Be$ neutron source

Only radiation experiments of configuration memory (static SEUs) were done. The DUT was placed 10 cm away from the neutron source. The results of irradiation runs are presented in Table 3.[8]

Table 3. Results of FPGA irradiation experiments with $^{241}Am/Be$ source

No	^{241}Am/Be source	water moderator	time [hours]	# SEUs
1	not present	not present	24	0
2	present	not present	24	9
3	present	present	24	2

8. CONCLUSIONS

The experiments proved radiation causes damages in electronic devices. Using this information there is a possibility to build system for measurements of radiation using Light Emitting Diodes and Charge Coupled Devices as a detectors.

Other thing are errors in Field Programmable Gate Array chips. Single Event Upsets are caused mainly by neutrons. Gamma radiation only limits the lifetime of devices but does not causes improper work. The results of investigations show that radiation mitigation methods should be used to ensure electronic system will work properly in the tunnel.

There are several methods of radiation mitigation[1]:

- Conventional shieldings.
- Chips dedicated to work in irradiation environment.
- Appropriate system design (eg. Triple Module Redundancy).

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