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Multichannel downconverter prototype for XFEL

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Streszczenie

Akceleratory cząstek są urządzeniami, w których cząstki elementarne przyśpieszane są do ultrarelatywistycznych prędkości. Wśród akceleratorów można wyróżnić grupę akceleratorów liniowych, w których cząstki poruszają się po linii prostej. Jednym z ich zastosowań jest tzw. laser na swobodnych elektronach (ang. Free Electron Laser - FEL), w którym energia elektronów przyśpieszonych do prędkości bliskiej prędkości światła zostaje przekształcona w emisję spójnego promieniowania elektromagnetycznego (promieniowanie synchrotronowe), wskutek hamowania w polu magnetycznym. Długość fali takiego promieniowania zależy od energii elektronów.

Dzięki takiemu promieniowaniu można badać budowę materiałów w skali atomowej, co jest wykorzystywane w wielu dziedzinach, od fizyki przez chemię i biologię po elektronikę. Umożliwia ono badania struktur tak małych, ak wirusy czy pojedyncze struktury białka, z nieosiągalną wcześniej dokładnością. W akceleratorze FLASH, działającym w ośrodku DESY w Hamburgu, udało się uzyskać promieniowanie o długości fali 6.5 nm. Obecnie planuje się budowę akceleratora XFEL, który będzie wytwarzać promieniowanie z zakresu Roentgena (0.085 6 nm).

W akceleratorze FLASH elektrony są przyśpieszane w nadprzewodzących wnękach rezonansowych w wyniku oddziaływania między cząstkami i zmagazynowanym polem elektromagnetycznym. Jest to oddziaływanie dynamiczne, bowiem pole wewnątrz rezonatora zmienia się w czasie, np. dla akceleratora FLASH częstotliwość zmian pola wynosi około 1.3 GHz. Właściwą amplitudę oraz fazę pola względem wiązki zapewnia system sterowania, dostarczając do wnęk odpowiednią moc i zapewniając optymalne warunki dla przyśpieszania elektronów.

Celem tej pracy, realizowanej w ramach współpracy Politechniki Warszawskiej z DESY, było zaprojektowanie układu przemiany częstotliwości (ang. downconverter), który jest jednym z kluczowych podukładów systemu sterowania. Układ ten służy do przetworzenia sygnału pochodzącego z wnęki rezonansowej, który to zawiera informację o aktualnej amplitudzie i fazie pola EM, do postaci umożliwiającej cyfryzację na potrzeby numerycznego kontrolera.

Projektowany układ musiał spełniać ostre wymagania przewidziane dla budowanego obecnie akceleratora XFEL a jednym z celów tej pracy było wyznaczenie kierunku rozwoju w badaniach nad optymalnym rozwiązaniem.

Wymagania dla układu przemiany częstotliwości dotyczyły głównie jak najmniejszych zniekształceń sygnału wskutek szumów i nieliniowości. Dodatkowo, projekt musiał zapewniać równoległą pracę ośmiu kanałów oraz być zwarty, tak by można go było łatwo przetestować w istniejącym akceleratorze. W procesie projektowania należało skonfrontować stawiane wymagania z możliwościami rzeczywistych układów i, w przypadku konfliktu, ustalić kompromis.

W pracy przedstawiono proces projektowania układu przemiany częstotliwości, od jednokanałowego prototypu po ośmiokanałową płytę VME. Głównym elementem układu przemiany częstotliwości jest mieszacz, który najsilniej wpływa na właściwości toru pośredniej częstotliwości. Zależnie od budowy, mieszacze możemy zaklasyfikować jako układy pasywne lub aktywne, a główne różnice dotyczą poziomu szumów oraz nieliniowości.

Praca ta miała pionierski charakter, gdyż nie można było na podstawie wcześniejszych badań w DESY zdecydować, jaki mieszacz pozwoli uzyskać najlepsze rezultaty. Dlatego też postanowiono poprowadzić badania dwutorowo i skonstruować prototypy z układami pasywnymi jak i aktywnymi. Pomiary układów prototypowych pomogły określić podstawowe parametry dla każdego z rozwiązań ale także poszerzyły naszą wiedzę na temat układu przemiany częstotliwości jako elementu systemu sterowania.

Następnym etapem, po układach prototypowych, było zaprojektowanie układu wielokanałowego, gdzie dodatkowo pojawiły się problemy wpływu przesłuchów między kanałami. W tej pracy omówiono projektowanie ośmiokanałowej płyty układu przemiany częstotliwości, wykorzystującej mieszacze aktywne.

Ze względu na doświadczalny charakter, oprócz realizacji podstawowych funkcji, projekt musiał umożliwiać łatwe zmiany w konfiguracji tak aby każdy z podsystemów mógł być niezależnie badany i optymalizowany.

Wymagania te udało się spełnić w zaprojektowanym ośmiokanałowym układzie, który przebadano najpierw w warunkach laboratoryjnych a następnie w akceleratorze FLASH.

Badania szumów takich układów są bardzo trudne, ponieważ wymagają specjalnego sprzętu i metod. W tym celu wykorzystano układ opracowany w DESY (F. Ludwig), który generuje sygnały o różnych częstotliwościach, które jednocześnie są w dużym stopniu skorelowane dlatego w wyniku mieszania tych sygnałów, w badanym układzie przemiany częstotliwości, następuje niemal pełna kompensacja szumów pochodzących z generatora odniesienia.

W pierwszej kolejności zmierzono podstawowe parametry układu przemiany częstotliwości, takie jak liniowość czy przesłuchy a następnie stabilność amplitudy i fazy pojęcia wprowadzone na potrzeby opisu właściwości układu przemiany częstotliwości jako podsystemu

akceleratora. Głównym sprawdzianem jakości zaprojektowanego układu był wynik pomiaru niestabilności energii wiązki, za pomocą pomiarów energii promieniowania synchrotronowego.

Uzyskane wyniki pozwalają sądzić, iż zaprojektowany układ może być użyty w głównej części nowego akceleratora XFEL, natomiast nie wiadomo jeszcze czy może być również wykorzystany w pierwszej sekcji, gdzie stawiane wymagania są znacznie ostrzejsze.

Interpretacja badań przeprowadzonych w akceleratorze FLASH, przy użyciu zaprojektowanego układu doprowadziła do weryfikacji dotychczasowych poglądów panujących w DESY co do podstawowych mechanizmów niestabilności i jednocześnie potwierdziła przeprowadzone niedawno symulacje. Dotychczas sposoby poprawienia jakości sterowania wiązką skupiały się na redukcji szumów wielkoczęstotliwościowych, jako najlepiej widocznych przebiegów na panelach systemu diagnostycznego. Wykorzystując nowy układ przemiany częstotliwości pokazano, iż szumy te nie oddziaływają na wiązkę, gdyż zostają odfiltrowane przez pasmowoprzepustową wnękę rezonansową oraz w wyniku działania pętli sprzężenia zwrotnego.

Drugi wniosek płynący z doświadczeń jest taki, iż największym problemem, w systemie kontroli nowego akceleratora, stanowić będą szumy typu 1/f, które są źródłem dryftów, a sposobów minimalizacji ich wpływu jest niewiele. Głównymi źródłami szumów 1/f są zarówno układ generacji sygnału odniesienia jak i sam mieszacz w układzie przemiany częstotliwości. Obecnie podejmowane są próby zmniejszenia wpływu tych szumów oraz dryftów temperaturowych za pomocą odpowiednich procedur kalibracyjnych, jednak prace te są jeszcze w fazie wstępnej.

Podsumowując, cel tej pracy, czyli zaprojektowanie układu przemiany częstotliwości dla nowego akceleratora, został wykonany i udokumentowany. Wyniki badań tego układu wyznaczają kierunek rozwoju układów przemiany częstotliwości, nie tylko dla akceleratorów FLASH czy XFEL ośrodka DESY ale także innych budowanych na świecie.

Wyniki tej pracy pierwsze ukazują pomiary kompaktowego rozwiązania układu przemiany częstotliwości, działającego w akceleratorze, w oparciu o koncepcję przewidzianą dla nowych akceleratorów i zostały opublikowane na dwóch międzynarodowych konferencjach: [1, 2].

Zaprojektowany układ służy już jako podstawa dla rozwijanego obecnie projektu zintegrowanego kontrolera, opartego o standard ATCA.

Multichannel downconverter prototype for XFEL

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Abstract

The development of Free-Electron Lasers entails stringent requirements for the stability of the accelerating fields what leads to the need for better control systems. The goal of this thesis was to design a part of the control system - the downconverter, which would fulfill the requirements foreseen for the new XFEL accelerator.

This thesis shows the design process of the high intermediate frequency downconverter. To achieve superior performance, many contradicting factors, especially noise and linearity, had to be compromised. Therefore, the development of the downconverter was based on two prototype boards, which used either passive or active mixer.

The knowledge obtained from the experiments with the prototypes was used in the design of the multichannel downconverter board, where the requirements set was extended by inter-channel crosstalk. The experiments, performed in the FLASH facility, were the first, which showed the performance of compact, high IF downconverter in the accelerator environment. They provided valuable data for further research and revealed that some sources of the disturbances were underestimated.

This thesis sets the goals for further downconverter developments and the results lead to the conclusions which will bear fruit in future works.

Acknowledgments

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List of Abbreviations

ACB - Advanced Carrier Board
ACC - Accelerating Module
ADC - Analog to Digital Converter
ATCA - Advanced Telecommunications Computing Architecture
BC - Bunch Compressor
BW - Bandwidth
CW - Continuous Wave
DAC - Digital to Analog Converter
DESY - Deutsches Elektronen-Synchrotron
DRO - Dielectric Resonator Oscillator
DSP - Digital Signal Processing/Processor
DWC - Downconverter
EM - Electro Magnetic
FEL - Free Electron Laser
FF - Feed-Forward
FLASH - Free Electron Laser in Hamburg
FPGA - Field Programmable Gate Array
FR4 - Fire Resistant material no. 4
HF - High Frequency
IF - Intermediate Frequency
IP3 - Third order intermodulation point
LLRF - Low Level Radio Freguency
LO - Local Oscillator
LSB - Least Significant Bit
MO - Master Oscillator
OA - Operational Amplifier
P1dB - 1 dB compression point
PCB - Printed Circuit Board
PLL - Phase Locked Loop
RF - Radio Frequency
RMS - Root Mean Square
SASE - Self Amplified Spontaneous Emission

SFDR - Spurious Free Dynamic Range

SIMCON - Simulator and Controller

SNR - Signal to Noise Ratio

VME - VERSAmodule Eurocard

VS - Vector Sum

XFEL - X-ray Free Electron Laser

Contents

Chapter 1

Introduction

Particle accelerator is a machine in which elementary particles, like protons or electrons, are accelerated in electromagnetic field almost to the speed of light. There are two basic constructions of accelerators, ring and linear. In ring accelerators particles move in circular trajectory, gaining energy with every single pass, while in linear accelerators particles are accelerated along straight line. One of the advantages of ring accelerators is their size, because the energy of the particle is increased with every single pass therefore linear accelerators, to obtain the same energy as ring ones, would require much more space. The advantages of linear accelerator derive from the fact that straight path do not require strong magnetic fields which are needed for changing the trajectory. Furthermore, linear accelerators do not suffer from synchrotron radiation problems and can accelerate heavy particles or ions.

This thesis is related with the development of FLASH, a linear accelerator located in Deutsches Elektronen-Synchrotron (DESY) research center in Hamburg. FLASH is Free Electron Laser (FEL), what means that the electrons accelerated to the ultra-relativistic speeds to obtain electromagnetic radiation in the process of Self Amplified Spontaneous Emission (SASE). Its high brilliance synchrotron radiation is exploited for many experiments.

There are numerous applications of FEL radiation and they cover many areas: physics, biology, chemistry or solid state engineering. First, FEL experiments allow accelerator physicists to confront the theory and measurement data. Many physical phenomenons can be investigated: SASE, interaction between electrons and photons, properties of synchrotron radiation and many more.

Second group of applications is related to the biology. With FEL radiation, scientists can investigate molecular structure of living organisms or drugs, because imaging of such

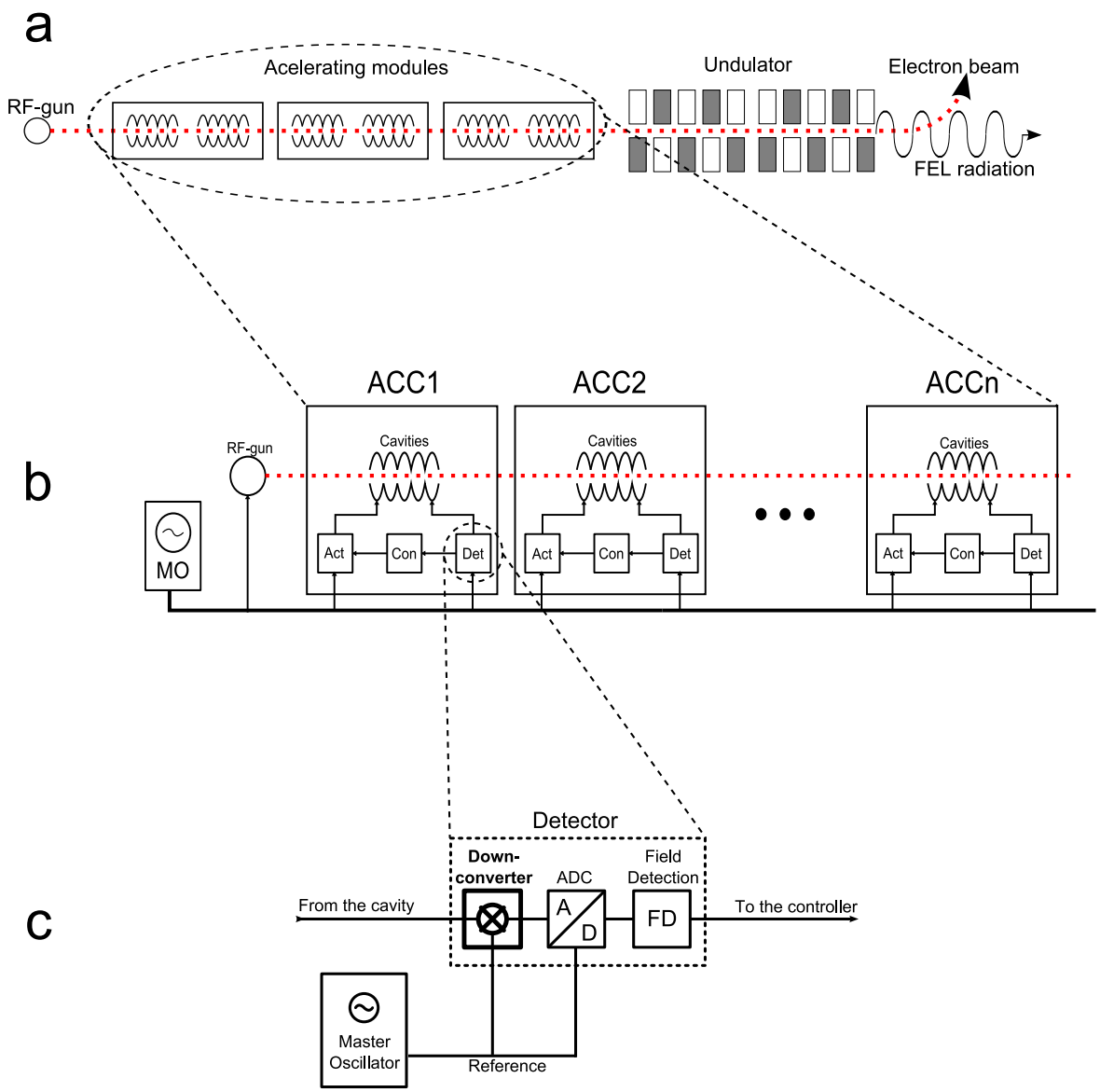

Figure 1.1: Location of the downconverter inside the accelerator: FLASH accelerator overview (a), details of the accelerating modules (b), the detector and its subcomponents (c).

small objects like viruses or proteins is possible. In chemistry, FEL radiation, because of short wavelength gives deep insight into the structure of nano-world. With FEL radiation it is possible to design new substance with atom-scale precision.

Simplified diagram of the FLASH facility is depicted in Fig. 1.1a. It consists of RF-gun for producing bunches of electrons, modules accelerating them in the EM field, and undulators, where the energy of the electrons is transferred to the synchrotron radiation in the SASE process.

Effectiveness of FEL depends on the appropriate control of the EM field in the accelerating module (ACC), shown in detail in Fig. 1.1b. Each module consists of eight cavities and a control system, which consists of detector (Det), controller (Con) and actuator (Act). The cavity is a superconducting resonant structure where the energy of the electric field is accumulated and then transferred to the electron beam. The field is probed inside the cavity and the analog signal is led to the detector, which transforms it to the numerical representation which is used then by the following controller. In the controller this signal is processed and the output signal is send to the actuator, which feeds the cavity with an appropriate driving signal. To provide right operation of the system, each module circuitry is synchronized with the reference, which is the Master Oscillator (MO). The main task of the control system is to provide assure appropriate amplitude and phase of the EM field and stabilize it over time.

This thesis focuses on the downconverter, which is a subcomponent of the detector, as depicted in Fig.1.1c. The detector consists of the downconverter, analog-to-digital converter (ADC), and field detection block. The high frequency signal, which comes from the cavity undergoes downconversion producing intermediate frequency signal what makes following digitization in the ADC possible. Finally, the numerical algorithm performs the field detection and the result is send to the controller.

The detector, described in this thesis, has been developed at DESY (Germany), for already described FLASH accelerator and its next generation successor XFEL. However, the developments of the detectors are carried in many institutions around the world ([1]): Lawrence Berkeley National Laboratory (LBNL, USA), Fermi National Accelerator Laboratory (FNAL, USA), Thomas Jefferson Lab National Accelerator Facility (JLAB, USA), KEK (Japan), and many universities and research centers from Europe, associated in the EuroFEL project.

This thesis resulted from close cooperation with many DESY people, especially Dr. Frank Ludwig, who was involved in developing other circuits, and is a continuation, on a higher level, of the author's Bachelor Thesis [3], which was published in March 2006.

The nature of this thesis is experimental, the design process of the multichannel downconverter is described and measurement results are presented. It is worth to mention, that the design of such devices is difficult, not only because of tight requirements but also because of interdisciplinary nature of work, fuzzy borders of each system, and strict time schedule. Due to the fact, that downconverter is the front-end of the detector, it is key element when considering the noise performance or linearity.

To design the downconverter, knowledge from many areas of science was required. Mostly from electronics but high energy physics was also needed. In electronics, the most important was analog RF/microwave design but the surroundings of the downconverter obliged the designer to understand problems of high speed digital circuits and control system as well as the technical details of manufacturing process.

It is necessary to emphasize, that control system has not been fully analyzed (especially noise issues), when work on this thesis had started therefore during the development of the downconverter some of earlier ideas have been revised. For example, at the beginning of the Author's work, a priority was to decrease the high frequency (HF) noise because it was believed that it is the most important contributor to the beam instability.

After some experiments performed with the downconverter, described later in this thesis, the role of HF component of the noise is much more understood. It came out that even though the HF noise is clearly visible on the diagnostic panels, it is mostly a display problem because it is not imposed on the beam due to cavity filter properties. On the other hand, the measurements revealed flicker noise problems, which were not considered before.

Another issue was, how to select the right intermediate frequency for the downconverter. The decision, which IF should be used has far-reaching consequences for all accelerator subsystems thus without it, the development was a bit of a leap in the dark. There are arguments both for increasing as well as for decreasing the intermediate frequency, but it is almost impossible to find the optimum, other than through measurements. IF considerations are described in Chapter 3.

Another idea, which was not experimentally proven, was the set-up for generation of the local oscillator (LO) signal, required for the downconverter operation (it determines the IF) which must be synchronized with the Master Oscillator. Generally, the set-up based on the frequency dividers and upconverter was proposed (F. Ludwig) but it was unclear if the additional noise from such set-up can be neglected. The details of LO signal generation are described in Chapter 5.

Beside conceptual problems, the Author of this thesis needed to overcome many obsta-

cles. The requirements for the field stability were very stringent: 10^{-4} in both amplitude and phase. To fulfill them, the downconverter had to provide extremely low noise and high linearity. Since these requirements contradict each other, a compromise had to be reached. The requirements for inter-channel crosstalk needed careful PCB design. The unsettled value of the IF called for downconverter to be designed in a such way to easily accommodate various elements or devices in case of its change.

This thesis is organized as follows. Chapter 2 gives a theoretical basis for description of signals and circuits, which are used in the low level part (LLRF) of the control system, putting emphasis on noise issues. Chapter 3 presents the analysis of the LLRF control system: the control loop is described in detail, the sources of errors are shown, the noise contribution of each subsystem to the overall noise performance is analyzed, and intermediate frequency considerations are carried out.

Chapter 4 describes the design process of the multichannel downconverter, while following Chapter 5 shows the results of the experiments made with the new downconverter. At the end, in Chapter 6 a summary of work is given along with some proposals for future work.

Chapter 2

Theory

The control system consists of various elements, which can be divided, concerning the signal on which they operate, into three groups: analog, digital, and mixed. The first group consists of such devices as amplifier, mixer or analog filter, where both input and output signal is purely analog. Second group contains devices which process only digital signals, like FPGA or DSP. In the third group, there are collected devices, which change representation of the signal: analog-to-digital and digital-to-analog converters.

The analysis of the control system requires appropriate models of signals and circuits. The goal of this analysis is to describe the instabilities, which derive from noise of the control system itself, and which act onto the EM field inside the cavity. Basing on this analysis appropriate steps can be taken, to minimize the influence of the disturbances and increase the stability of the field.

In the following sections, the description was limited to signals and circuits, which exist in the control system of the accelerator.

2.1 Signal modeling

Generally, signals can be classified as deterministic or stochastic. Consequently, while deterministic signals can be exactly described in any instant of time, the stochastic ones are random, thus they can be predicted with certain doze of probability.

The description of a signal results from model (deterministic or stochastic), which is applied to describe certain phenomena. To fully describe the deterministic signal, complete set of its parameters is needed while the description of the stochastic process uses statistical measures.

In practice, signals (e.g. noisy sine-wave) contain both deterministic and stochastic

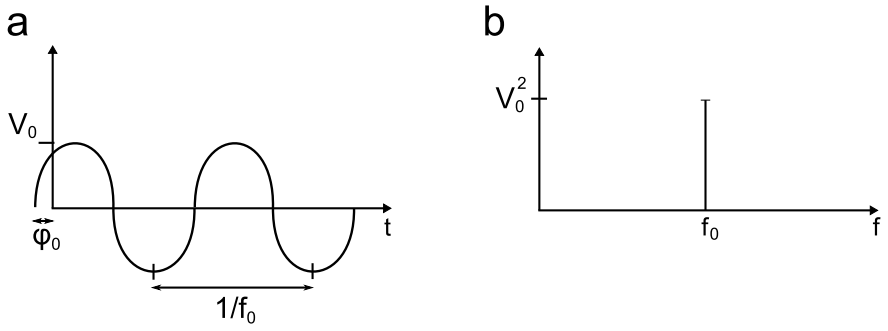

Figure 2.1: Deterministic sinusoidal signal in the time domain (a) and its representation in the frequency domain (b).

components. The easiest way to describe such signal is to decompose it into deterministic and stochastic component and describe each with appropriate model.

Usually, depending on the ease of use or measurement aspects (e.g. accuracy), signals can be described both in time and frequency domain. In the time domain such terms as amplitude, root-mean-square (RMS) value, or jitter are used while in the frequency domain signals are described with power, spectral density, or integrated jitter.

The deterministic, sinusoidal signal, $v(t)$, can be described, in time domain, as follows:

$$v(t) \quad = \quad V_0 \cos(2\pi f_0 t + \varphi_0), \tag{2.1}$$

where V_0 is the amplitude, f_0 is the frequency, and φ_0 is the phase. Since all the parameters of the signal do not change over time, this signal is called stationary one. Fig. 2.1 shows two the representations of the $v(t)$ signal: in the time domain (a) and in the frequency (spectrum) domain (b). The recent one is obtained by applying Fourier transform ($\mathcal{F}\{x\}$) to the signal. Unfortunately, because of noise and distortions, in the real world deterministic signals do not exist.

In the real world, only stochastic signals exist and can be measured. The description of a stochastic signal bases on the deterministic form. Any fluctuating sinusoidal signal $v(t)$ can be described as follows:

$$v(t) \quad = \quad V_0[1 + \alpha(t)] \cos(2\pi f_0 t + \varphi(t)), \tag{2.2}$$

where V_0 is the amplitude, f_0 is the frequency, while $\alpha(t)$ and $\varphi(t)$ represent the amplitude and phase variations of the signal, respectively. The quantities $\alpha(t)$ and $\varphi(t)$ are called the amplitude and phase noise respectively and as such are independent from each other.

When both noise contributions are small enough i.e. $|\alpha(t)| \ll 1$ and $|\varphi(t)| \ll 1$, $v(t)$ can be approximated as follows [4]:

$$v(t) = V_0 \cos(2\pi f_0 t) + V_0\, \alpha(t) \cos(2\pi f_0 t) - V_0\, \varphi(t) \sin(2\pi f_0 t). \tag{2.3}$$

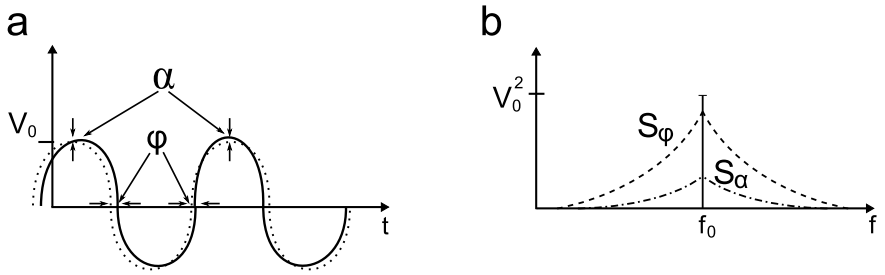

Figure 2.2: Noisy sinusoidal signal in the time domain (a) and its representation in the frequency domain (b).

Fig. 2.2 depicts $v(t)$ both in time (a) and frequency (b) domain. In the time domain, the noisy signal (solid) is shown at the background of the noiseless one (dots). The fluctuations of the amplitude or phase (jitter) are clearly visible in the points where sine wave reaches its extrema or at zero crossings respectively.

In the frequency domain, the spectrum $\mathcal{F}\{v(t)\}$, consists of three components: the carrier frequency f_0, the amplitude noise sidebands S_α, and phase noise sidebands S_φ, which correspond with appropriate time domain components in the (2.3).

Because the measurements in the frequency domain are much easier to perform, it is more common to express the amplitude and phase noise in the frequency domain, for instance using double sideband power spectral density $S(f_m)$, which is defined as follows [5][6]:

$$\begin{aligned} S_\alpha(f_m) &= \frac{\alpha^2_{rms}(f_m)}{\mathrm{BW}_\alpha} \ \frac{\mathrm{V}^2}{\mathrm{Hz}} \\ S_\varphi(f_m) &= \frac{\varphi^2_{rms}(f_m)}{\mathrm{BW}_\varphi} \ \frac{\mathrm{rad}^2}{\mathrm{Hz}} \end{aligned} \tag{2.4}$$

where $f_m = f - f_0$ is the offset frequency, and BW_α and BW_φ represent the measurement bandwidth and are assumed to be enough narrow to consider S_α or S_φ constant inside the relevant one.

Common term, when describing phase noise, is the $\mathcal{L}(f_m)$ which is the ratio of power density in one sideband per Hz bandwidth at an offset frequency f_m away from the carrier to the total signal power, as depicted in Fig. 2.3. $\mathcal{L}$ is usually presented in logarithmic scale and expressed in dBc/Hz [5]. It is usually assumed that single sideband

$$\mathcal{L}(f_m) \simeq \frac{S_\varphi(f_m)}{2} \tag{2.5}$$

but this assumption is only valid for signals where $|\varphi(t)| \ll 1$ [5].

For detector testing purposes, a figure of merit, called amplitude and phase stability, is introduced. Stability is defined over certain bandwidth $(\mathrm{f_2} - \mathrm{f_1})$ by an appropriate

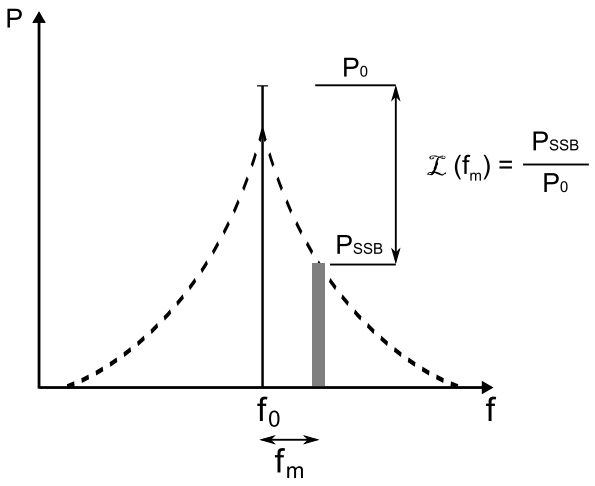

Figure 2.3: Definition of $\mathcal{L}(f_m)$.

integrals as follows [7]:

$$\left(\frac{\Delta A}{A}\right)_{rms} = \sqrt{\int_{f_1}^{f_2} S_\alpha(f)df} \tag{2.6}$$

$$\Delta\varphi_{rms} = \sqrt{\int_{f_1}^{f_2} S_\varphi(f)df} \tag{2.7}$$

Unfortunately, the direct use of the definition above is difficult in practice, therefore, for the laboratory use, equivalent definitions have been introduced in the measurement chapter.

When concerning the detector (or downconverter) as a part of the synchronization system, integrated timing jitter is commonly applied. It is defined as follows [7]:

$$\Delta t_{rms} = \frac{1}{2\pi f_0}\sqrt{\int_{f_1}^{f_2} S_\varphi(f)df}, \tag{2.8}$$

2.2 Circuit modeling

The detector itself is the source of noise which disturbs the cavity probe signal thus reducing the field measurement accuracy. In this section, the modeling of disturbances, introduced by the detector components, will be shown. The detector's (Fig. 1.1c) critical components, for noise performance, are the downconverter, which contains mixer and amplifier, and the analog-to-digital converter.

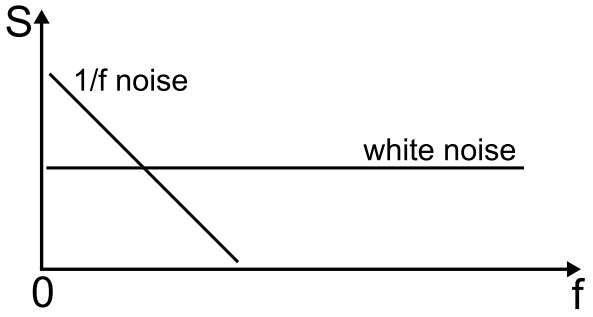

Figure 2.4: Power spectral density of white and 1/f noise.

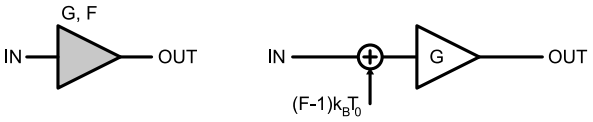

Figure 2.5: Noisy amplifier (left) and its equivalent circuit (right).

The noise introduced by the amplifier can originate from many physical phenomena. For simplicity, in this section only white and flicker noise will be considered. The white noise originates from the random movement of electrons in the conductor in any temperature above 0 K. Therefore white noise is also known as thermal noise. In the frequency domain, the power spectral density (PSD) of the white noise is flat up to very high frequencies (Fig. 2.4).

The flicker noise is also called 1/f noise, because its power spectral density increases at low frequencies with the reciprocal of the frequency, as depicted in Fig. 2.4. It originates from slow phenomenas like changes in a conductive channel, slow changes in the semiconductors, or aging processes.

Noisy amplifier can be decomposed into two parts, noiseless amplifier and additional noise source, as depicted in Fig. 2.5. The contribution of the amplifier noise can be observed as extra amplitude noise, phase noise or flicker noise. Modeling the noise of the amplifier can be carried out using power spectral density of the amplitude or phase noise, which are described as follows [7],[4]:

$$S(f) = b_0 + b_{-1}\frac{1}{f} \tag{2.9}$$

where b_0 represents the white noise contribution, b_{-1} is experimental coefficient, P_{in} is the input power, T_0 is the room temperature and k_B is the Boltzmann constant. b_0 is defined as follows:

$$b_0 = \frac{Fk_BT_0}{P_{in}}. \tag{2.10}$$

while b_{-1} is equal to the power spectral density at 1 Hz ([7]).

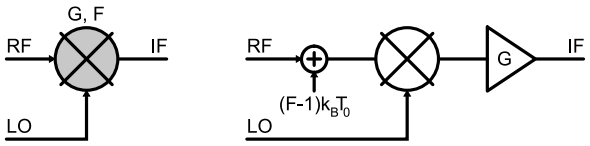

Figure 2.6: Noisy mixer (left) and its equivalent circuit (right).

Noise in mixers is modeled similarly to the amplifiers, as depicted in Fig. 2.6. Mixers' equivalent circuit consists of a noiseless mixer, responsible for frequency conversion, an amplifier, representing conversion gain (or loss), and a noise source, which represents additional noise, introduced by the mixer.

In the time domain the mixer performs the multiplication operation on two input signals, called RF and LO. Therefore, the output (IF) signal is described as follows:

$$v_{\mathrm{IF}}(t) = v_{\mathrm{RF}}(t) \cdot v_{\mathrm{LO}}(t). \tag{2.11}$$

Assuming noisy sinusoidal input signals (see 2.2):

$$v_{\mathrm{RF}}(t) = A_{\mathrm{RF}}\,(1+\alpha_{RF}) \cdot \sin(2\pi f_{\mathrm{RF}} t + \varphi_{\mathrm{RF}}(t) + \varphi_0) \tag{2.12}$$

$$v_{\mathrm{LO}}(t) = A_{\mathrm{LO}}\,(1+\alpha_{LO}) \cdot \sin(2\pi f_{\mathrm{LO}} t + \varphi_{\mathrm{LO}}(t)) \tag{2.13}$$

the output signal of a downconverter can be rewritten to the following form:

$$v_{\mathrm{IF}}(t) = \frac{A_{\mathrm{RF}} \cdot A_{\mathrm{LO}}}{2} \cdot (1+\alpha_{RF})(1+\alpha_{LO}) \cdot \cos(2\pi(f_{\mathrm{RF}} - f_{\mathrm{LO}}) + \varphi_{\mathrm{RF}}(t) - \varphi_{\mathrm{LO}}(t) + \varphi_0) \tag{2.14}$$

As one can see, noise on the mixer output can origin from two input ports. To simplify the analysis it is assumed that LO port works in saturation, what means that LO input signal large enough to switches the internal active devices (diodes, transistors). This assumption allows to neglect considering the amplitude noise of LO signal thus making LO port sensitive only to phase noise. The RF signal is small so both amplitude and phase noise contribute to the IF output. In such conditions, the phase noise on the IF output origins from RF and LO inputs, while the amplitude noise origins from RF port only:

$$v_{\mathrm{IF}}(t) = \frac{A_{\mathrm{RF}}}{2} \cdot (1+\alpha_{RF}) \cdot \cos(2\pi(f_{\mathrm{RF}} - f_{\mathrm{LO}}) + \varphi_{\mathrm{RF}}(t) - \varphi_{\mathrm{LO}}(t) + \varphi_0) \tag{2.15}$$

Generally, the phase noise of the IF signal can be described in the frequency domain, using power spectral density, as [8]:

$$S_{\varphi,\mathrm{IF}}(f) = S_{\varphi,\mathrm{LO}}(f) + S_{\varphi,\mathrm{RF}}(f) - 2\,\gamma(f)\sqrt{S_{\varphi,\mathrm{LO}}(f) \cdot S_{\varphi,\mathrm{RF}}(f)} \tag{2.16}$$

where $\gamma(f)$ is the correlation factor, describing correlation between LO and RF noise and ranges from –1 to 1. Important conclusion now can be derived, the mixer output noise can be reduced when using correlated signals. When the signals are uncorrelated ($\gamma(f) = 0$), the above equation can be written as:

$$S_{\varphi,\mathrm{IF}}(f) = S_{\varphi,\mathrm{LO}}(f) + S_{\varphi,\mathrm{RF}}(f). \tag{2.17}$$

Above equation may be extended by the component representing internal mixer noise $S_{\varphi,\otimes}(f)$, which is also assumed to be uncorrelated with both signals:

$$S_{\varphi,\mathrm{IF}}(f) = S_{\varphi,\mathrm{LO}}(f) + S_{\varphi,\mathrm{RF}}(f) + S_{\varphi,\otimes}(f) \tag{2.18}$$

Analog reasoning can be carried out for the propagation of the amplitude noise, with exception that LO noise is not transferred to the IF output:

$$S_{\alpha,\mathrm{IF}}(f) = S_{\alpha,\mathrm{RF}}(f) + S_{\alpha,\otimes}(f). \tag{2.19}$$

where $S_{\alpha,\otimes}(f)$ is additional mixer amplitude noise.

The noise description using power spectral density is advantageous to the noise figure based description. PSD gives more insight into the source of noise because it allows to distinguish between white and flicker noise and also to decompose noise into amplitude and phase components.

The last noise contributor is the the analog-to-digital converter. There are three sources of the ADC noise: front-end noise, clock jitter and quantization noise. The noise performance of the ADC can be easily summarized by signal-to-noise ratio (SNR) [9]:

$$\mathrm{SNR} = -20\log_{10}\left[(2\pi f_{in} t_j)^2 + \frac{2}{3}\left(\frac{1+\epsilon}{2^N}\right)^2 + \left(\frac{2\sqrt{2}V_n}{2^N}\right)^2\right]^{\frac{1}{2}} \tag{2.20}$$

where: f_{in} is the analog input frequency of fullscale input sinewave in [Hz], t_j is the rms value of the combined clock jitter (internal and external) in [s], ϵ is the average differential nonlinearity in [LSB][1], N is the number of bits, and V_n is the rms value of the effective input noise voltage in [LSB]. In perfect conditions ($t_j = 0, \epsilon = 0, V_n = 0$), the above equation can be simplified to the well-known formula [9]:

$$\mathrm{SNR} = 6.02N + 1.76 \text{ dB} \tag{2.21}$$

The noise contribution from each source can be now analyzed. The first component depends on the input frequency and clock jitter. One can see that increased frequency

[1]Size of the Least Significant Bit of the ADC

of the input signal decreases the SNR. Increasing the sampling frequency also degrades SNR, not only because the performance of the whole ADC circuit degrades but also the clock jitter becomes more important. Clock jitter, t_j, is the sum of two uncorrelated jitters, external clock jitter and internal ADC added jitter. Because, usually, the fist component dominates, low phase noise clock signals are needed. However, it is hard to maintain clock signal purity when increasing the frequency. The bandwidth of the clock input of the ADC is assumed twice the sampling frequency unless additional filtering on clock input is used [9].

Second component of (2.20) accounts for nonlinearities of the ADC. Since it decreases with the number of bits it is worth to use precise ADCs. The last component of (2.20) refers to the noise of the ADC front-end and depends on the design of the ADC. For sine-wave input, the rms of the input noise can be calculated from the SNR as follows [7]:

$$v_{\text{rms}} = V_{\text{FS}} \cdot 10^{-\frac{\text{SNR}}{20}} \quad [\text{V}] \tag{2.22}$$

where V_{FS} is the full scale voltage of the ADC.

In this chapter the modeling of signals and circuits for the needs of the detector was shown. In the next one the analysis of the control system will be presented.

Chapter 3

Control system

The electron beam is accelerated by the electric field, accumulated in the cavity. Since, in FLASH, this field varies over time the efficiency of the acceleration process is highest when the beam is injected into the cavity when the electric field reaches its maximum. The purpose of the control system is to synchronize cavity field with the beam to assure optimal beam conditions.

The control loop is depicted in Fig. 3.1. From the control theory point of view, it is a classical feedback loop system composed of a cavity, detector block, controller unit, actuator block, and synchronization system (Master Oscillator). The cavity RF field is probed and the signal containing information about its instantaneous amplitude and phase is processed by the detector and than used to control this field. This processing is based on a controller's algorithm, which compares actual parameters of the detected signal with their desired values (set-point) and produces an appropriate signal for actuator to correct the field. The synchronization system is based on the reference signal generated

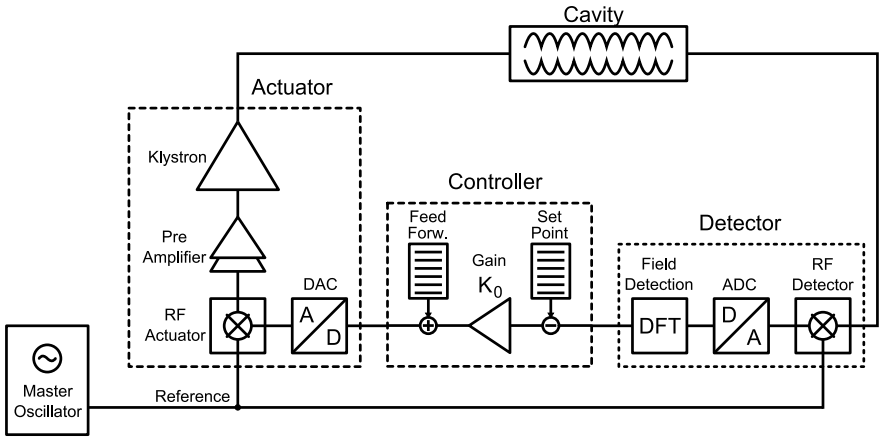

Figure 3.1: The control loop.

by the Master Oscillator to provide a set of signals for proper timing of each device in the accelerator [10].

The detector block consists of the Radio Frequency detector, analog-to-digital converter (ADC) and a field detection algorithm. The electric field inside the cavity is probed with an antenna (not shown) and transmitted through a coaxial cable to the detector. Cavity probe signal has the same frequency as the field inside the cavity and for FLASH it is about 1.3 GHz. This signal undergoes downconversion to the intermediate frequency (IF) in the RF detector. The output signal from RF detector has much lower frequency, thus it can be sampled by the ADC. The digital signal from the ADC is then numerically processed using a field detection algorithm, yielding information about the actual amplitude and phase of the cavity field. This data is compared in the controller with the relevant data stored in the set-point table. The resulting signal (error signal) is amplified by K_0 and added to the feed-forward table(FF). The output signal from the controller passes then to the actuator, where it is converted back to the analog form in the digital-to-analog converter (DAC). After upconversion in the RF actuator to the cavity resonant frequency and amplification in a multistage preamplifier and high power klystron, it drives the cavity.

3.1 Disturbances

Many factors affect the signals in the control loop therefore the control system must counteract this disturbances, because they influence the field, and consequently beam energy, stability. The nature of the disturbances can be either deterministic or stochastic what leads to different correction techniques.

Phenomena	Origin			Model	
	Mechanical	Electrical	Thermal	Deterministic	Stochastic
Noise		×			×
Drifts		×	×	×	×
Crosstalk		×			×
Microphonics	×				×
LF detuning	×	×		×	

Table 3.1: Classification of the disturbances in the control system according to their origin and nature.

The major disturbances, in the control system, are electrical noise, drifts, crosstalk,

microphonics, and Lorenz-force (LF) detuning. They are categorized in Table 3.1. Classifying disturbances by their origin leads to three groups: mechanical, which are related to changes in the shape (dimensions) of the cavity; electrical and thermal. Some of the disturbances, like noise and microphonics, have random nature, others (Lorenz-force detuning and some drifts) can be predicted to some degree.

Electrical noise results from random processes, which occur in conductors and semiconductors. In the control system of FLASH, the biggest contributors are white and flicker noise [11]. Thermal noise, or white noise, is introduced by any lossy electric component and its contribution to the system depends on the bandwidth. This noise is responsible for signal degradation and influences measurement accuracy. Flicker noise appears in electronic components (resistors, capacitors) and semiconductor devices (diodes, transistors). Unlike the white noise, which spectrum is flat up to very high frequencies, the power spectral density of the flicker noise is concentrated at low frequencies, because it originates from slow changes in the devices' structure. The influence of the flicker noise on the control system is still investigated but it seems that it is responsible for unwanted fluctuations of beam energy in the milisecond range. [11]

Next unwanted effects are temperature drifts. Temperature influences all parts of the control system, but mostly cables and analog electronic devices. Temperature affects electrical length of coaxial cables which connect cavity with the detector thus causes phase variations of RF signal. Radio frequency devices, like mixers or amplifiers, are based on semiconductor devices though they are very sensitive to temperature. The influence of the temperature drifts is usually done with temperature stabilization of crucial components but such solution is very expensive and cannot be applied in the distributed systems, therefore drift calibration techniques are being developed [11].

Next source of errors is crosstalk, which appears due to the electric or magnetic coupling between systems or channels and results in unwanted (in particular place) signals. In the control system the most difficult to counteract is crosstalk between RF signals coming from different cavities because of the exact same frequency as the signal of interest.

The mechanical disturbances, which detune the cavity are Lorenz-force detuning and microphonics. The effect of detuning is depicted in Fig. 3.2. With no detuning present, the resonant frequency of the cavity $f_0 = 1.3$ GHz (solid line). Detuning (dashed line) shifts resonance peak in the amplitude characteristic (Fig. 3.2a) to f_1 while the cavity is still stimulated with 1.3 GHz. This effect results in higher attenuation at f_0 and also shifted phase (Fig. 3.2b) [12].

Lorenz force detuning results from high gradients of the electric field inside the cavity

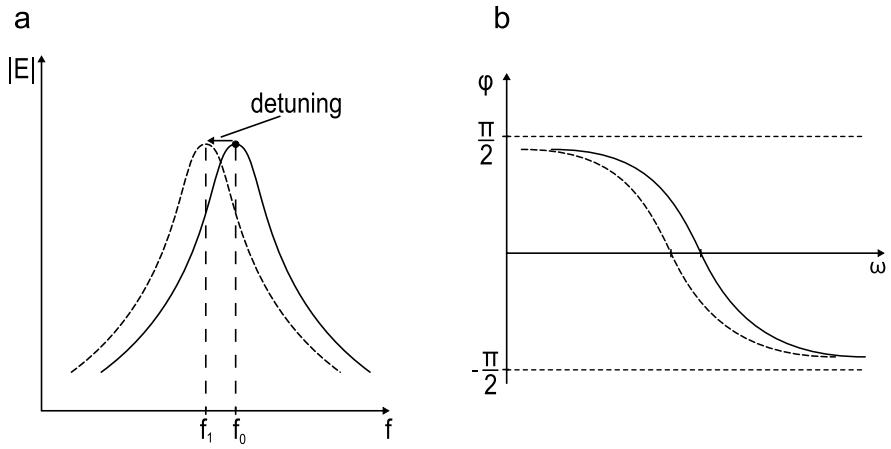

Figure 3.2: Illustration of detuning influencing amplitude (a) and phase characteristic (b) of the cavity: nominal (solid) and detuned (dashed).

(~ 25 MV/m) and produces predictable detuning effect. The influence of Lorenz force detuning can be reduced by appropriate control algorithms and/or active piezoelectric drivers, which mechanically counteract the changes of the cavity shape.

Microphonics originate from mechanical components movement (e.g. vacuum pumps) and ground vibrations and, unlike the Lorenz-force detuning, have stochastic nature. They affect the shape of the superconducting cavity, which bandwidth is very narrow (432 Hz, $Q_L \sim 3 \cdot 10^6$), significantly changing its resonant frequency. Microphonics are relatively slow (BW $<$ 1 kHz), but due to their random nature, only feedback based control loop can reduce their influence.

3.2 Analysis of the control loop

The properties of the control loop can be analyzed with a control theory approach, using model depicted in Fig. 3.3. The control loop is here modeled using separate blocks of cavity, detector and controller, each described with an appropriate transfer function in the Laplace domain with the complex argument $s = \sigma + j\omega$ [7]. This model includes also sources of primary disturbances describing the detector noise R(s), Master Oscillator noise M(s), actuator noise A(s) and cavity disturbances D(s).

The cavity output signal Y(s), shaped by the cavity transfer function G(s), undergoes downconversion and consequently the phases of the signal and the reference signal M(s), are subtracted and the detector disturbances R(s) are added to the IF signal. Then, the IF signal is shaped by the detector transfer function C(s) and the resulting signal Y'(s) is subtracted from the set-point W(s). The resulting error signal E(s) is then shaped by

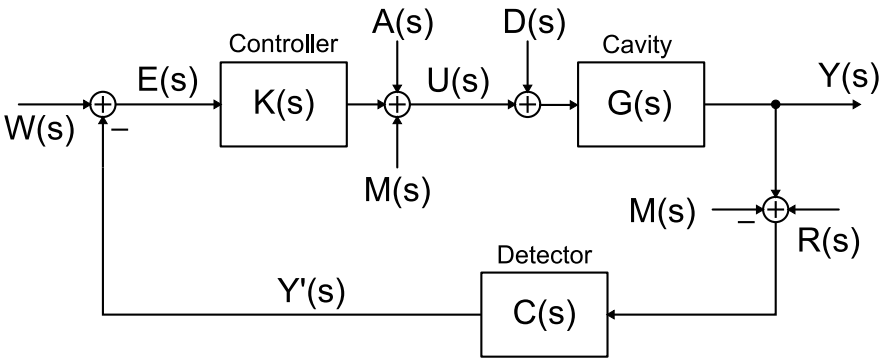

Figure 3.3: Control theory model of the control loop.

the controller characteristic K(s). Finally, the phase of the Master Oscillator is added as a result of the upconversion and actuator noise A(s) and mechanical disturbances D(s) are added.

Since this model focuses on the analysis of signals lying close to the carrier, all transfer functions are described in baseband. The cavity transfer function G(s) is shifted from 1.3 GHz to 0 and modeled with a low-pass filter function:

$$G(s) = \frac{\omega_{12}}{s + \omega_{12}} \tag{3.1}$$

where $\omega_{12} = 2\pi \cdot 216$ Hz is the pulsation corresponding to half of the cavity bandwidth. The detector transfer function C(s) is described also with a low-pass transfer function:

$$C(s) = \frac{\omega_c}{s + \omega_c} \tag{3.2}$$

where $\omega_c = 2\pi \cdot 1$ MHz represents the detector bandwidth. The controller K(s) is described by the frequency independent gain K_0.

The cavity signal Y(s) can be expressed with [7]:

$$Y(s) = H_A(s)\ [D(s) + A(s)] + H_W(s)\, W(s) + H_R(s)\, R(s) + H_{MO}(s)\, M(s) \tag{3.3}$$

where

$$H_A(s) = \frac{G(s)}{1 + G_0(s)} \tag{3.4}$$

$$H_W(s) = \frac{G(s)K(s)}{1 + G_0(s)} \tag{3.5}$$

$$H_R(s) = -\frac{G_0(s)}{1 + G_0(s)} \tag{3.6}$$

$$H_{MO}(s) = \frac{G(s)}{1 + G_0(s)} + \frac{G_0(s)}{1 + G_0(s)} \tag{3.7}$$

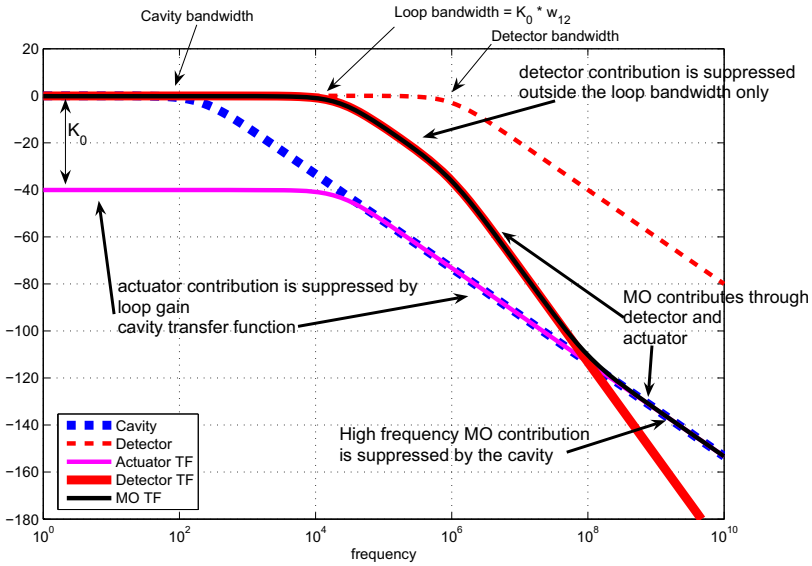

Figure 3.4: Transfer functions constituting the cavity response Y(s) (3.3), for $K_0 = 100$.

are the transfer functions of the actuator, set-point, detector, and Master Oscillator respectively, while

$$G_0(s) = G(s) \cdot K(s) \cdot C(s), \tag{3.8}$$

is the transfer function of the open-loop.

The results of the analysis of (3.3) are presented in Fig. 3.4, for the gain $K_0 = 100$. This figure depicts the transfer function of each noise contributor, as well as the cavity G(s) and detector C(s) characteristics. Due to 216 Hz cut-off frequency and the gain $K_0 = 100$, the loop bandwidth extends up to 21.6 kHz.

The actuator contribution (noise and mechanical disturbances) is suppressed by the feedback inside the loop bandwidth and by the cavity filter function outside it. The detector and MO contributions are suppressed only outside the loop bandwidth. The Master Oscillator contribution consists of two components, first comes from the detector, where MO signal is used in the downconversion process, second from the actuator, where the MO signal is used for the upconversion. Since at low frequencies the detector component dominates, the MO contribution follows the detector curve. At high frequencies, the MO contribution follows the actuator curve, dominating over the detector contribution.

The analysis leads to the following conclusions. When the controller gain is small, the cavity field is influenced mostly by the actuator noise (dominating over the detector noise in the absolute measure) and disturbances. Increasing the gain results in stronger suppression of the actuator contribution what leads to improved field stability. However, with father gain increase, the loop bandwidth broadens, thus suppression of the detector

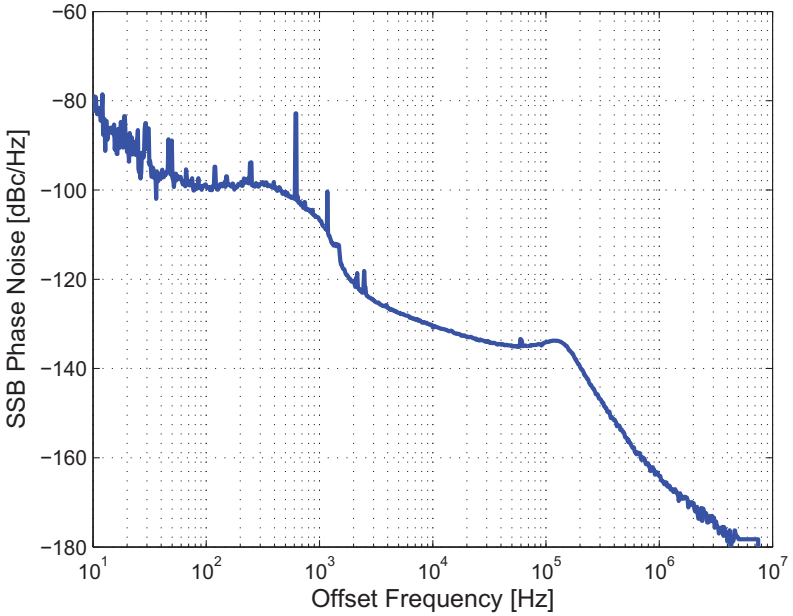

Figure 3.5: Master Oscillator phase noise [13].

contribution starts on higher frequencies. This leads to higher amount of detector-sourced noise in the loop and thus the stability decreases. This effect was verified experimentally and presented in Chapter 5.

Fig. 3.5 depicts phase noise characteristic of the Master Oscillator installed in FLASH. Basing on this data simulations of the control control loop were performed [7]. The results are depicted in Fig. 3.6. One can see, that the cavity field follows the Master Oscillator signal at the low frequencies. The explanation lies in the is the feedback based controller as it minimizes the error signal, which results from subtracting the cavity and MO phases. At higher frequencies, the cavity effectively filters out the MO noise, and the cavity no longer follows the MO but the cavity phase is then dominated by the detector noise. As it is seen in Fig. 3.6, the noise contribution of the actuator is negligible because of the suppression by the feedback.

The amount of noise introduced by the detector partially depends on the noise figure of the downconverter what was the reason for using low noise devices in the DWC design. The results of the simulations described above, appeared recently and showed that the contribution of the downconverter to the whole system is not as important as it was assumed. The results showed that the most effective way to decrease the detector contribution is to reduce its bandwidth. This is realized using averaging consecutive samples in the digital part of the controller.

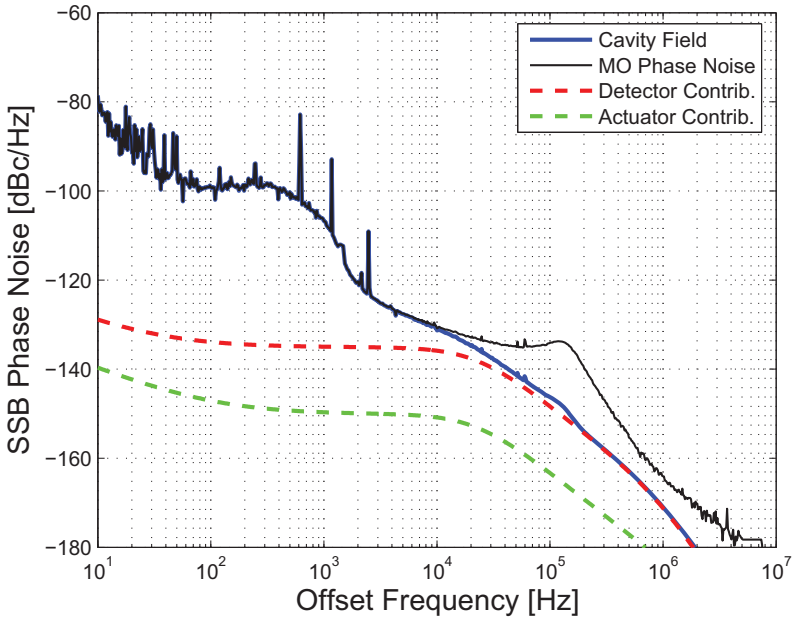

Figure 3.6: Simulation based contribution of each system to the cavity field. [7]

3.3 Processing the IF signal

The control system of FLASH, shown in Fig. 3.1, exploits a conversion of the RF cavity signal to an intermediate frequency signal. While other solutions are possible, like baseband or direct sampling [7], this section will focus on two of them, called 'IQ sampling' and 'IF sampling'. First is currently used in FLASH while second is a development system foreseen for XFEL.

The 'IQ sampling' scheme is depicted in Fig. 3.7 and it is a practical realization of the system described previously in Fig. 3.1. It uses time-domain switched LO signal (phase keying) which is generated by shifting the phase of 1.3 GHz reference signal by 90° every 1 μs. In the downconverter the IF signal of 250 kHz is produced as a result of mixing of this LO and the probe signals. Fig. 3.8a depicts the time domain representation of an IF signal, which is then sampled by the ADC. Fig. 3.8b shows the complex representation of this signal. The in-phase (I) and quadrature (Q) components of this signal are determined with the field detection algorithm by simple addition of the appropriate detected signal voltages:

$$\begin{aligned} S_1 + S_2 &= (+I, +Q) + (-I, +Q) = (0, 2Q) \\ S_2 + S_3 &= (-I, +Q) + (-I, -Q) = (-2I, 0) \end{aligned}$$

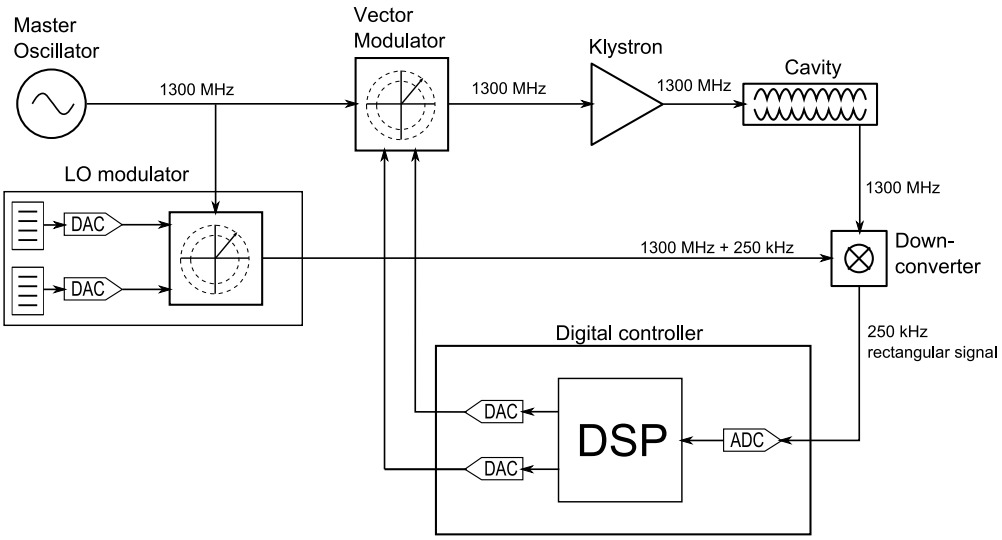

Figure 3.7: IQ sampling scheme.

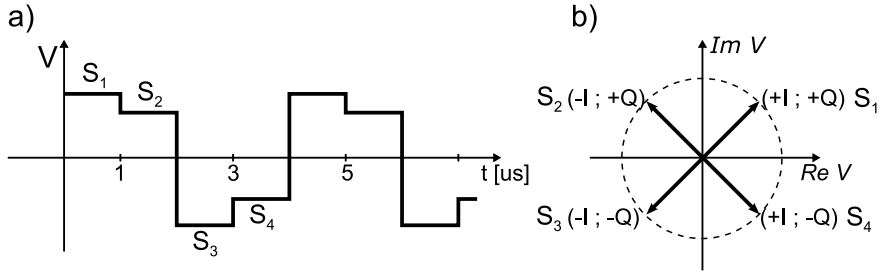

Figure 3.8: Ideal time domain 250 kHz rectangular signal (a) and its complex representation (b).

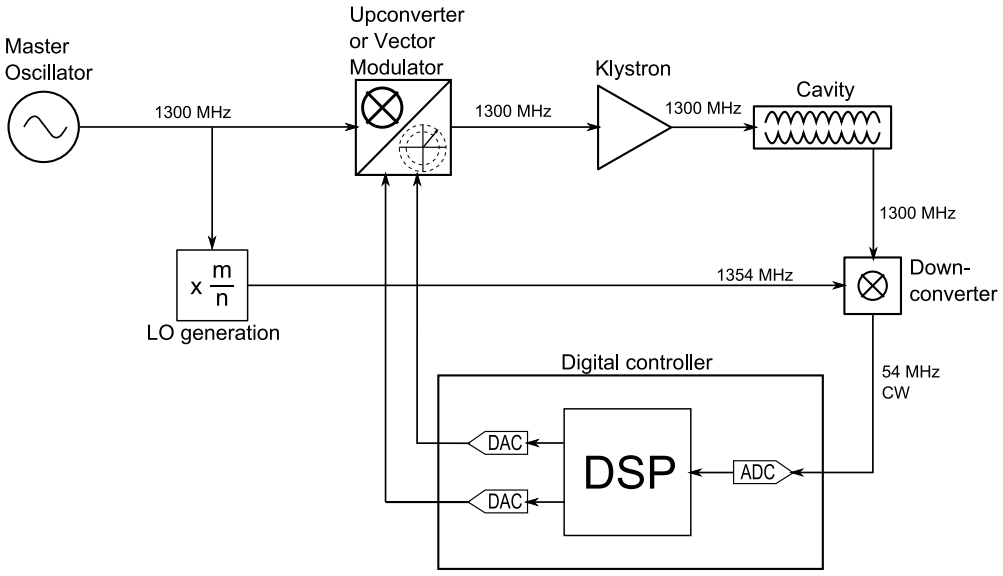

Figure 3.9: IF sampling scheme.

In the 'IF sampling' scheme, depicted in Fig. 3.9, the LO and consequently the IF signals are continuous waves. 'IF sampling' has been foreseen to operate at higher IFs; experiments range from 9 to 54 MHz but the final decision has not been made yet [14][15]. The LO signal is generated by fractional dividing frequency the MO reference signal. The LO generator will be described in detail later, as it plays major role in the noise budget. The LO signal is mixed with the cavity probe signal in the downconverter, producing continuous-wave of the intermediate frequency. The IF signal is then sampled by the ADC as it was in the previous scheme while the field detection algorithm works differently depending on the intermediate and sampling frequencies.

The 'IF sampling' scheme has its advantages and disadvantages; it offers better filtering possibilities because at high frequencies filters do no need require high values of inductance or capacitance. Furthermore,the IF allows to get rid of baseband distortions, like 50 Hz spikes from power supply or switching voltage regulators as well as crosstalk from timing and synchronization signals that are strongly present in the accelerator environment. The CW continuous wave signals can be easily observed with such measurement devices like spectrum analyzers or signal source analyzers, while in the switching scheme the only available tool is usually an oscilloscope. An high IF gives also an opportunity to collect more samples than actually needed for field detection and lowering the noise effects by averaging. Besides, high frequency system are less prone to the latency based problems [16].

Against the 'IF sampling' scheme speak mostly the ADC as high speed ADCs have lower bit resolution than their slow counterparts. Also the performance of the ADC (SNR, SFDR, etc.) decline with increasing of the frequency of the input signal. Furthermore, high speed ADCs need high quality clock signals because clock jitter adds to the input signal jitter. All those drawbacks can become less important with advancements of the ADC technology. Perhaps in few years there shall be available fast and more precise ADCs what will result in improved field detection.

3.4 Controlling a cavity set

For simplicity reasons, the control system discussed in the previous sections (Fig. 3.7 or Fig. 3.9) embraced one cavity only. Extending such system would require the use of one klystron and one controller per cavity what would result in a very high cost. To overcame this problem the vector-sum (VS) based systems are used. In vector-sum based system one high power klystron is employed for driving a set of cavities and their EM field is

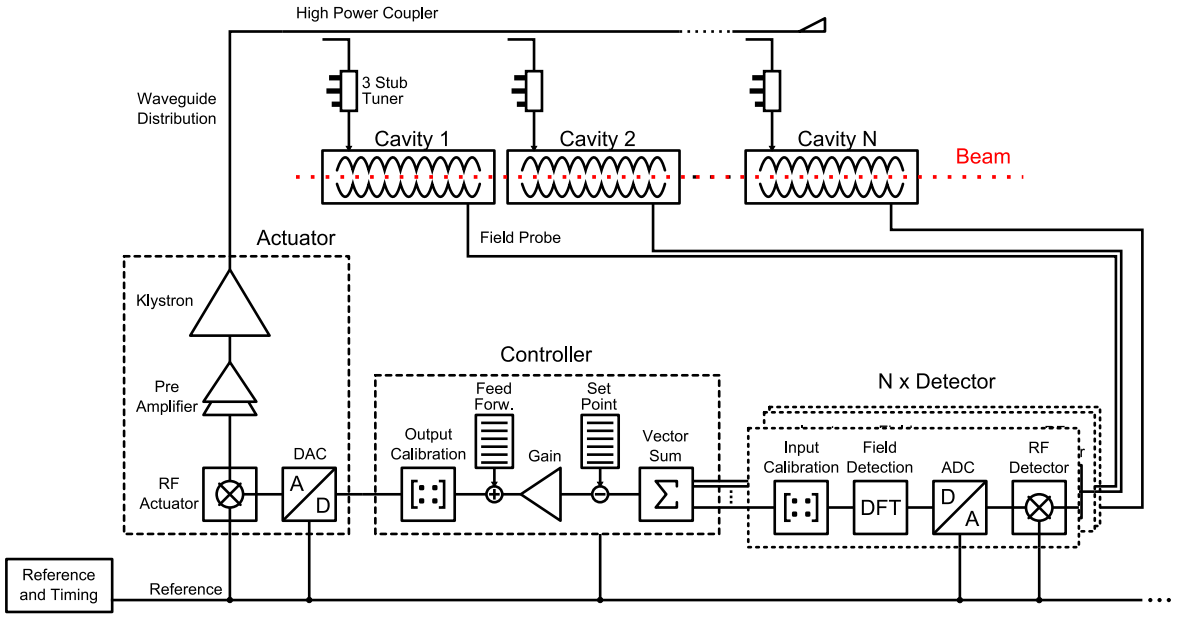

Figure 3.10: Vector sum based LLRF control loop.

stabilized using one controller [12].

The vector-sum concept refers to the fact that the effective voltage accelerating the electrons is an integral of voltage along the beam trajectory [12]. The probed signals can be utilized to approximate this integral with a sum of vectors representing the field inside each cavity along the beam line. Recovering of the vectors requires knowledge of the relationship between the vector field in each cavity and the magnitude and phase of the detected signal. These relationships are determined during the vector-sum calibration procedure, which enables to remove the influence of different cable lengths and attenuation from cavity to the detector output. Once the relationship is known, one can retrieve the appropriate vector representing the field inside the cavity.

Fig. 3.10 shows vector sum based LLRF control system. It is a generalized version of the system depicted in Fig. 3.1 and it fits to the real FLASH system where N=8. Eight cavity probe signals are downconverted and then sampled by ADCs, then field detection algorithm is performed on raw data producing eight IQ pairs. Cable length (from each probe to the appropriate ADC) is adjusted numerically, by multiplying the input signal by an appropriate coefficients from the rotation matrix[1]. The matrix coefficients are obtained in the vector sum calibration procedure. Next step is making the vector sum, where the advantage of the IQ representation over Aφ representation is visible.

[1]Name origins from the fact that in the IQ plane changing the phase is equivalent to the rotation of the vector.

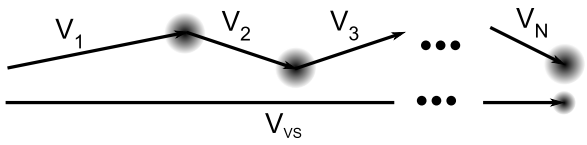

Figure 3.11: Vector sum and its components.

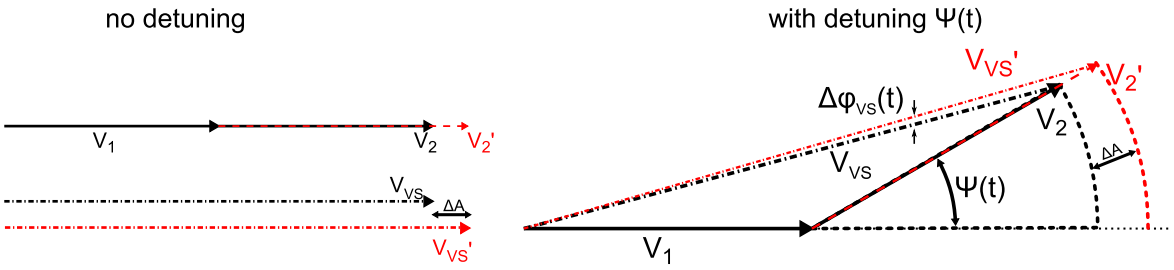

Figure 3.12: Vector-sum calibration – constant amplitude error.

Fig. 3.11 shows the field vectors and their vector sum. Basing on the VS principle, the controller stabilizes the vector sum while the field vector in each cavity fluctuates, due to distortions. Vector sum fluctuations are reduced by the loop gain and further by a $\sqrt{N}$ due to summation of stochastic quantities.

Although vector-sum based system reduces the overall cost of the accelerator it is also source of errors, which reduce the field stability. The most accurate procedure for vector-sum calibration utilizes the beam that absorbs the accumulated energy and a small drop down of the probed voltage serves as a convenient. It assumes that the field excited by the passing beam has the same strength in every cavity and is induced in the same time [17]. The VS calibration procedure uses high charge bunch which excites the field in the cavity. During the calibration the control loop is set to feed-forward operation only because otherwise the feedback would reduce the excitation effect. The cavity's transient response are equalized in amplitude and phase for all cavities during an iterative process. The details of VS calibration and its errors are described in [17, 7].

Main source of errors, in the vector-sum calibration procedure, are microphonics, as they introduce time dependent detuning $\psi(t)$. With perfect VS calibration slow disturbances, would be suppressed, by the loop gain (see Fig. 3.4) so increased gain would reduce error and improve the accuracy. However, any error during calibration leads to time dependent error component induced by the disturbances. This time dependent component can not be suppressed by the feedback and thus limits the overall performance of the system. The effects of conversion amplitude errors to phase errors and vice versa (AM/PM conversion) in the vector-sum system are shown in Fig. 3.12 and Fig. 3.13.

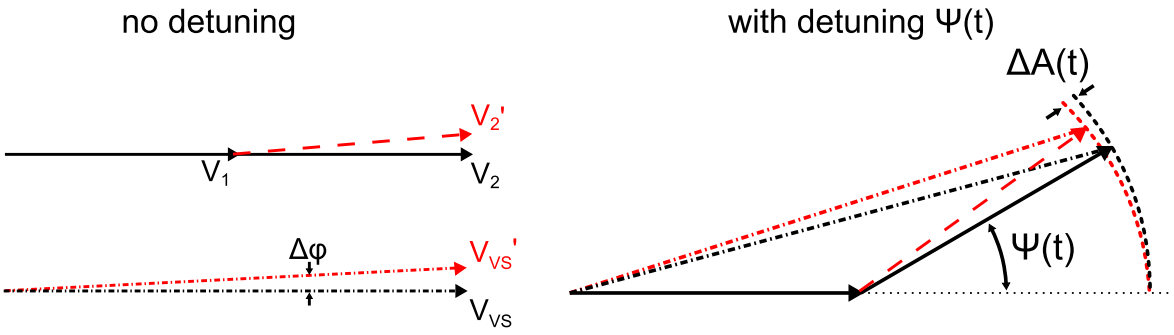

Figure 3.13: Vector-sum calibration – constant phase error.

Fig. 3.12 shows an influence of the time invariant amplitude error. For simplicity let us consider system with two cavities. Thus the vector sum V_{VS} is composed of two vectors, in which V_1 is treated as the reference (assumed constant) and V_2 is the vector indicating field in the second cavity. When no detuning is present, an amplitude error ΔA in the calibration leads to inaccurate recovering of the V_2 vector (labeled as V_2') and consequently to inaccurate vector sum V_{VS}'. For small detuning $\psi(t)$ the amplitude error ΔA remains constant but a time dependent phase error $\Delta\phi_{VS}(t)$ is introduced. Time dependency of this additional phase error results from time dependent detuning, while its magnitude depends on the magnitude of the amplitude error.

Similar situation arise when an influence of the phase calibration error in is considered – Fig. 3.13. With no detuning, any phase calibration error leads to constant vector sum phase error $\Delta\phi$. For small detuning angles, an additional time dependent amplitude error $\Delta A(t)$ is introduced. The time dependence of this error results form dime dependent detuning, while its magnitude depends on the magnitude of the phase error [17, 7].

The vector sum operation assumes the linearity of the detector therefor the linearity of the downconverter results from required vector sum accuracy [17]. To illustrate this let us consider the following example, showing how the nonlinearity of the detector can affect the vector-sum based system.

The vector sum is performed on two cavities. First operates with gradient of 12 MV/m, second with 24 MV/m, thus the total gradient is 36 MV/m. Assume the disturbance, which affects the first cavity, resulting in the gradient increase to 13 MV/m. The controller stabilizes the vector sum, so when the detector is linear, it will reduce the driving signal for the klystron thus the power delivered to each cavity. This will lead to 12.5 MV/m and 23.5 MV/m and the VS=36 MV/m. When the detector is nonlinear, for example because of gain compression, its output signal will be smaller than if it was linear so the controller will barely see the difference and will drive cavities to e.g.

12.75 MV/m and 23.75 MV/m resulting in VS of 36.5 MV/m. This means that the beam will experience higher total gradient as the disturbance was not suppressed.

Chapter 4

DWC design

Development of high IF downconverter was the main goal of the project. The new downconverter should fulfill stringent requirements for XFEL, defined by physicists. This chapter describes the design process, from requirements, through concept and prototype to final multichannel board.

The principle of measurement of the cavity field is depicted in Fig. 4.1. It is based on the assumption, that the electric field $\vec{E}$ induces RF voltage signal $\hat{V}_{RF}$, which is proportional to the magnitude of the electric field. This voltage is processed in the detector to obtain numerical values (A, φ), which correspond to the amplitude and phase of the electric field.

The XFEL requires 10^{-4} stability of the effective accelerating field (vector-sum from eight cavities). From the field stability requirements the parameters of corresponding detector output signal are derived; the field stability corresponds to amplitude and phase stability of 0.01% and 0.01° respectively [7].

From the downconverter point of view, the field stability has to be translated to the requirements put upon the IF signal $\hat{V}_{IF}$. The downconverter is the first subsystem of the

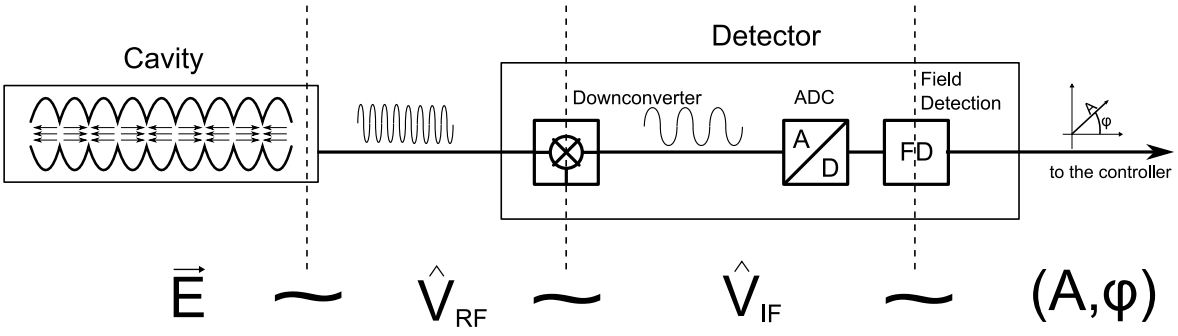

Figure 4.1: Measurement of the EM field.

detector thus its parameters strongly influence the signal of interest. The requirements for downconverter embraced noise, nonlinearity, crosstalk, drifts and some technical and compatibility issues.

Because the IF signal must be digitized, its noise can be easily expressed using the signal-to-noise ratio. The value of 10^{-4} corresponds to SNR of 80 dB and can be recalculated for total rms noise voltage at the ADC input using (2.22). Next requirement was linearity higher than 50 dB. Crosstalk from separated channels has to be lower than –80 dBc. Drifts were not defined in absolute measure, but it was assumed that they should be kept as low as possible.

Non electrical requirements included power, versatility, compactness and cost. The power of the DWC input signals (RF and LO) has to be minimized because in multichannel application the demand for high power involves power amplifiers, which introduce additional noise, nonlinearities, drifts, etc. The versatility requirement was added for first versions, mostly because of undefined intermediate frequency but also to efficiently use time and money. The design has to be compact, what means that its installation in the machine should be easy. Furthermore, space occupied by the downconverter must to be minimized, because future plans assume integration of DWC with the controller on single ATCA carrier board. The designer has to keep in mind that in the XFEL will contain more than 300 accelerating modules and similar amount of downconverters will be needed, therefore the cost of single DWC should be minimized.

The requirements described above were defined at very first stage of DWC design. With time, our knowledge of the control system grown and the requirements were modified. Because it was though that the downconverter strongly contributes to the noise budget, low noise of the DWC was the highest priority. The SNR-based calculation was replaced with more detailed analysis, which distinguish between amplitude and phase noise, but still as low noise as it can be achieved principle applied. Later, it appeared that the ADC is the biggest noise contributor and dominates the noise from the downconverter.

The influence of nonlinearities on the beam stability was unclear, therefore it was assumed to use high linearity devices. Generally, it was decided to build the new downconverter design as good as it can get to show that the downconverter is not the limiting factor in the control loop.

Fig. 4.2 depicts a general scheme of the downconverter block as a part of the detector. The downconverter consists of a mixer, filter and low noise amplifier (LNA). The mixer is stimulated with the attenuated cavity probe signal and pumped with the LO signal from

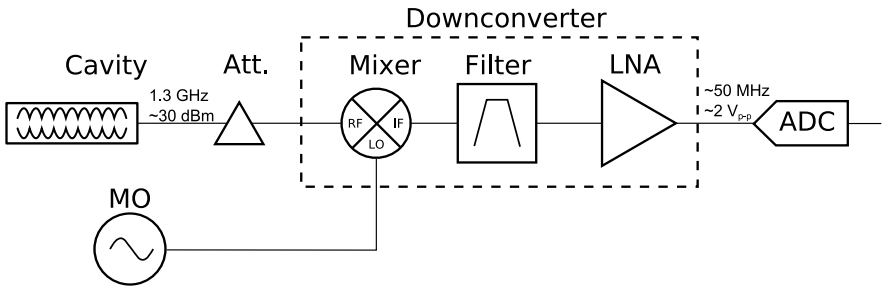

Figure 4.2: Block diagram of the downconverter.

the Master Oscillator. The output IF signal is then filtered to remove unwanted mixing products and amplified in the LNA to accommodate the signal to optimal voltage range of the ADC.

First decision which had to be made concerned mixer selection. Because of the limited space (VME 6U size C) it was decided to use integrated mixer circuit in a surface mounted case. Next issue was mixer type, which can be either passive or active. In principle, passive circuits are less noisy but require higher LO power to fully drive internal switching circuit and a LNA to compensate the conversion loss (the LNA can be discarded but this requires higher RF input power). Furthermore, they feature lower isolation between ports what results in high crosstalk.

Active mixers require less power and due to the conversion gain allow to abandon the amplifier. They also provide high linearity and good isolation. However, they are more noisy and require additional voltage source, what in high precision applications requires the use of low noise voltage regulator.

When the DWC project started, the role of the downconverter as a part of the control system was to be investigated. The simulations did not offer reliable prediction of the circuit behavior because of the complexity of the accelerator systems. Therefore, it was decided to base the search for optimal downconverter on prototype designs. The lack of knowledge about which of the requirements can be traded off, made the design process somehow intuitive. It was decided to design two prototypes, based on different mixer type and compare their performance. Although it was expected that the passive DWC will provide better overall performance it was decide to produce also low power active solution which could be used in the main section of the accelerator where the performance can be traded for size and cost, while passive solution could be used in the injector section where the performance is crucial and cannot be traded off.

After mixer market overview [18] the following ICs have been proposed: HMC483 from Hittite Inc. [19] for passive solution and LT5527 from Linear Technology Corp. [20]

Parameter	HMC483	LT5527
type	passive	active
noise factor [dB]	9	14
typ. RF input power [dBm]	20	0
LO power [dBm]	0*	-3
input IP3 [dBm]	33	24
conversion gain [dB]	-9	2
isolation [dB]	20	43

Table 4.1: Comparison of selected parameters of passive and active mixer ICs. * - see text

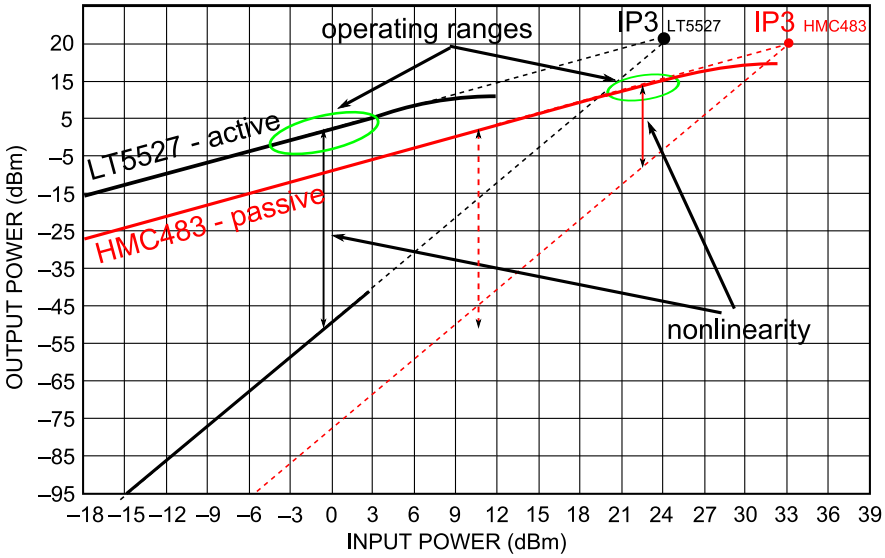

Figure 4.3: Output versus input power for active and passive mixer.

for active one. Basic parameters of these two chips are summarized in Table 4.1. To avoid problems with high LO power, required by passive mixers, selected HMC483 has internal buffer amplifier, therefore it requires only 0 dBm LO power while internal mixer circuit operates around 25 dBm. Unfortunately, suspicion appeared later, that such amplifier can introduce additional noise, discarding the low noise advantages of the passive mixer [21].

For better comparison, dynamic characteristics of bot mixer ICs has been drawn in Fig. 4.3, basing on the manufacturer's data [19, 20]. One can see that, because of the conversion loss, the passive chip requires more RF input power to obtain the same output power as its active counterpart. Therefore, the LT5527 operates at 0 dBm RF power while the HMC483 needs at least 10 dB more. However, the HMC483 can handle higher

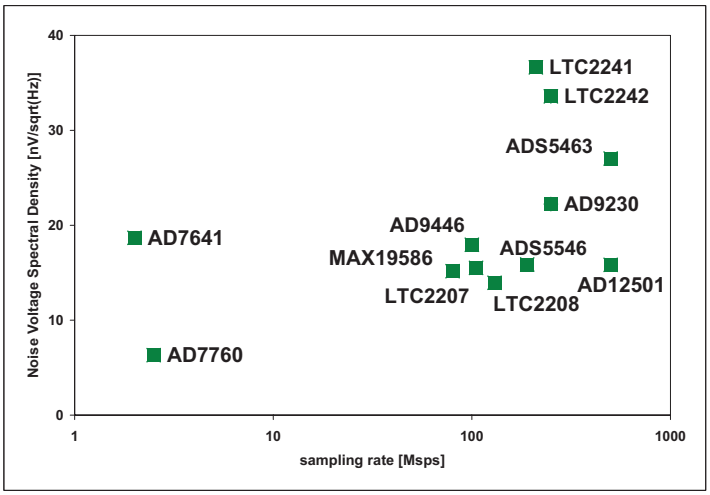

Figure 4.4: ADC market overview.

power of 20 dBm, providing about 12 dBm of output signal, making the IF amplification needless.

The nonlinearities are depicted as a vertical arrows, representing the distance between fundamental and third order intermodulation. At the operating ranges (green ellipses) the active chip represent much better linearity than passive. Although this comparison is done in different output conditions, shifting horizontally the arrow, representing LT5527 nonlinearities, to HMC483 curve, shows (dashed arrow) that still active chip is more linear.

The isolation of the device is crucial when comes to the crosstalk requirements. Crosstalk (leakage), usually, originates from electromagnetic coupling or finite isolation. The EM coupling occurs when two signal paths are routed in close proximity and the signals can transfer through capacitive or inductive coupling. To prevent this situation layout must be done with high care, signal layers shall be separated with ground planes and transmission lines should have good ground assured.

Finite isolation is typically an effect of non-ideal components, since every real-world device features finite isolation or directivity. There are two ways of providing high isolation. The first one requires the use of appropriate subcomponents, if there are such. The other one relies on increasing attenuation between channels, but this decreases also the signal power and results in higher noise figure. Therefore, attenuators can be employed un the system, once there is enough power to compensate for signal drop down.

As it came out during design, the ADC is the biggest noise contributor in the detector. Selection of an appropriate chip was done by M. Hoffmann and is described in [7]. Fig 4.4 depicts the overview of the contemporary ADCs, available on the market, as the noise

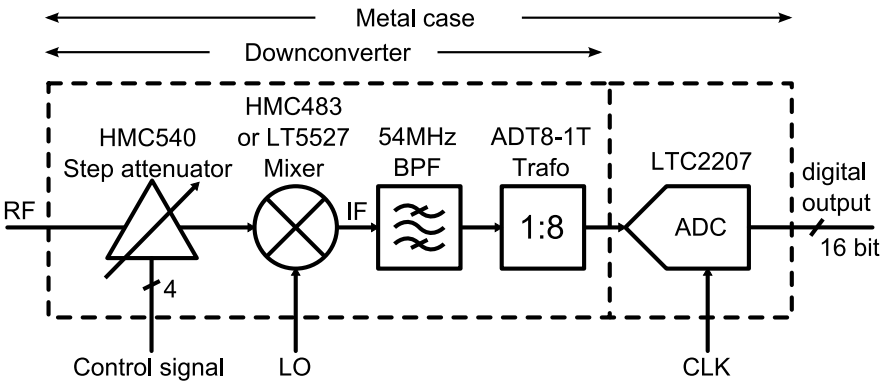

Figure 4.5: Block diagram of the DWC prototype.

performance versus sampling frequency. Three major groups can be distinguished: slow, high speed and direct sampling. The first group consists mostly of ΣΔ–ADCs, which are relatively slow ($f_s \sim 1 - 10$ MHz)[1] but very precise ($N \geq 18$) and introduce little amount of noise. Second group consists of high speed devices ($f_s \sim 100$ MHz) which are not so precise ($12 \leq N \leq 16$) and are more noisy. Last group contains direct sampling circuits ($f_s \sim 500 - 1000 +$ MHz), which have lowest bit number and introduce the biggest amount of noise. Furthermore, direct sampling units require special care when designing PCB and receiving data. Inside each group the noise performance is comparable thus reducing the overall ADC noise contribution leads either to the usage of slower devices or wait for further ADC technology development.

For high IF sampling scheme, it was decided to use the ADC from the second group. LTC2207 from Linear Technology yields 105 Msps sampling rate with 16 bit encoding and 78 dBFS of SNR at 900 mW dissipated power [22].

4.1 Prototype circuit

The detailed solution of the downconverter prototype is presented in Fig. 4.5. It consists of step attenuator (HMC540), mixer (HMC483 for passive and LT5527 for active solution), IF filter, and 1:8 step-up transformer. According to 'as good as it can get' rule, it was decided to integrate the downconverter and the ADC, excluding IF signal transmission problems, thus showing the performance limits of such configuration.

At the input, the step attenuator was added for experimental purposes. It allows to easily adjust the operating point of the following mixer. The selected filter was 3rd order Chebyshev, 10% bandwidth, 50 Ω matched, bandpass, from TTE Inc. [23].

[1] f_s – maximum sampling frequency

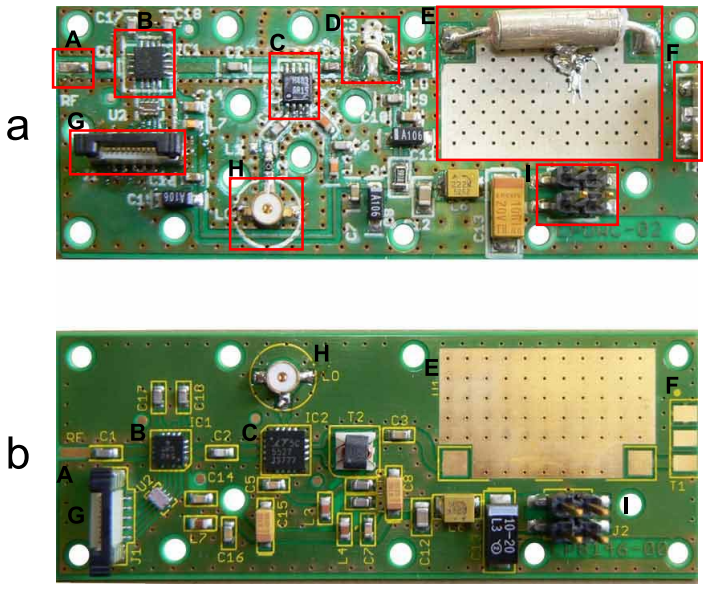

Figure 4.6: Downconverter prototype boards with passive (a) and active (b) mixer ICs. A - RF connector, B - digital attenuator, C - mixer, D - IF amplifier (shorted / not present), E - filter (shorted / not mounted), F - step-up transformer (part / not mounted), G - connector for attenuator control, H - LO connector, I - power supply connector.

The parameter of interest of the IF signal is voltage, because of the ADC, which measures it. Therefore, instead an amplifier, the step-up transformer was used to adjust the IF voltage to ADC full scale (1 dBFS). The transformer changes the ratio between voltage and current and, unlike the amplifier, does not introduce additional noise. Furthermore, the band-pass characteristic of the transformer can be exploited as an extra filter. The usage of the transformer had to be verified because it raises the input impedance for the ADC, from 50 to 400 Ω while the manufacturer recommends impedance lower than 100 Ω.

The prototype version of DWC was produced in two configurations: using passive mixer chip HMC483 (by M. Hoffmann) and active with LT5527 (by the author). In both version the same filters were used and the same ADCs (ADC boards by M. Hoffmann). The downconverter and the ADC were realized on two, separated PCBs[2] to reduce the noise coupling from digital circuits to sensitive analog RF part. Both boards were put into a metal case, providing good ground connection, low resistance path for the imbalance currents and serving as a EM shield, protecting the circuit from external distortions.

The downconverter boards are depicted in Fig. 4.6 for the passive (a) and active (b) ICs. The first PCB has been equipped with an additional IF amplifier (ERA series

[2]Printed Circuit Board

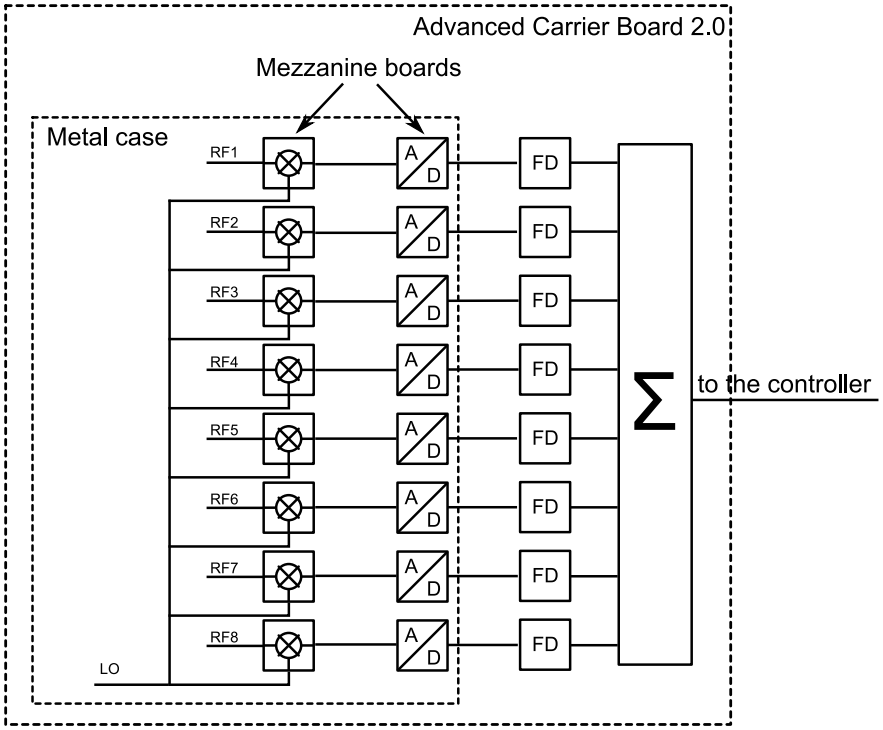

Figure 4.7: Scheme used for vector-sum operation using prototype DWCs.

from Mini-Circuits), which could be used in case the ADC did not work properly with high impedance transformer. In both cases almost the same power supply system was used; it consists of low noise voltage regulator (on separate board) and LC (inductors and capacitors) ladder for additional filtering. Both solutions were designed in a way that they work with the same ADC board (designed by M. Hoffmann). The LO signal distribution was realized through coaxial cables because of limited space (233×160mm).

Because the controller used in FLASH (SimCon 3.1) is integrated with ADCs (14-bit) it is not possible to use it with the prototypes. Therefore, exclusively for prototype DWCs, a special board, called Advanced Carrier Board (ACB 2.0) has been designed (by P. Strzalkowski). Fig. 4.7 depicts an application where ACB serves as a motherboard for DWC and ADC boards, performs field detection and sends the vector sum data, through optic link, to the controller. ACB also assures synchronization and controls digital attenuators and ADCs. Fig. 4.8 depicts a part of the realization of this concept.

There was a few month interval between manufacturing passive and active version of the downconverter. The experimental results of passive DWC measurements, on which further DWC developments were based, can be found in [7]. Because of the delay, the measurement time foreseen for the active DWC coincided with time reserved for multi-channel DWC (described in the following section). Therefore, the measurements of the

Figure 4.8: DWC prototype boards and ADC boards in the metal housing.

active prototypes were made cursorily, just to prove the principles, while the emphasis was put on the multichannel circuit (results in Chapter 5)

4.2 Multichannel downconverter

Multichannel downconverter design had to meet not only the requirements for prototypes but also it had to be compatible with the old DWC version. In this section the details of designing multichannel downconverter will be described. Main difficulties will be discussed as well as proposed solutions.

The design is based on the active DWC prototype, described above. Fig 4.9 depicts the schematic of a single channel. It consists of the input stage, filtering stage, IF amplifier, output stage and power supply section. Each stage will be described in detail in the following sections. To isolate sensitive RF devices from low frequency power supply distortions every mixer has its own, low noise voltage regulator (from +15 to +5 V). For all IF amplifiers only two voltage regulators (from +15 to +5 V and from -15 to -5 V) were used since they have quite good Power Supply Rejection Ratio (PSRR) [24].

The input stage of the downconverter consists of a mixer (LT5527) with an appropri-

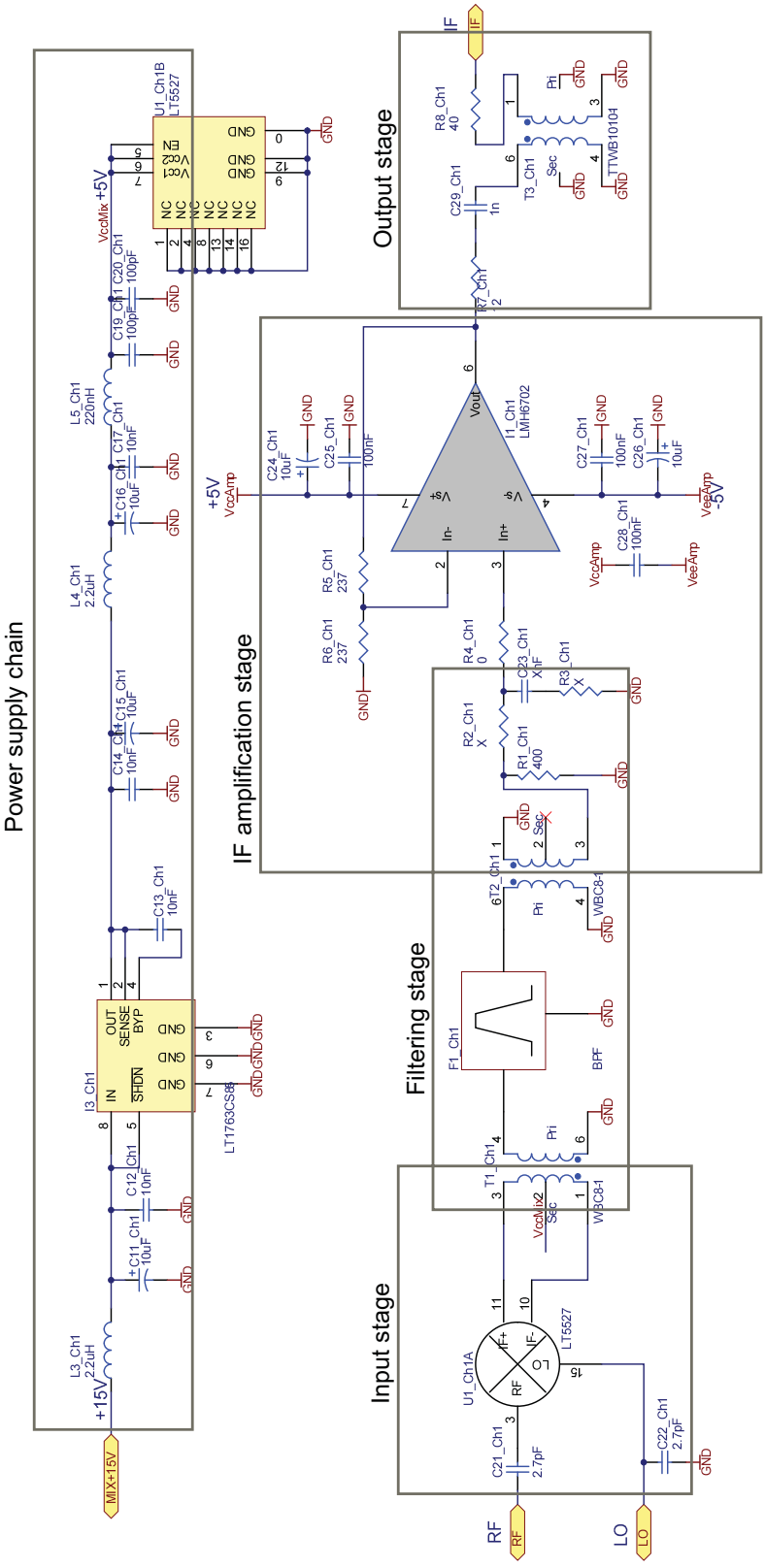

Figure 4.9: Single channel of VME downconverter.

ate matching circuits on its RF, LO and IF ports, designed basing on the manufacturer's data. The IF port was matched using a transformer, according to the Linear Inc. recommendations. The transformer on the IF port performs three functions: transforms high output impedance of IF port, converts differential IF port to single-ended input of the following filter, and enables biasing the mixer. The WBC8-1 Coilcraft transformer was used [25], with impedance ratio of 8:1, what converts 400 Ω mixer output impedance to 50 Ω for the following filter.

The IF filtering is performed with a custom-made LC filter from TTE Inc. [23]. Two versions have been foreseen: band-pass (10% BW, $f_c = 54\ MHz$, 50 Ω, Bessel type), and to give an opportunity to experiment with various IF, a low-pass ($f_c = 54\ MHz$, 50 Ω, 3rd order Chebyshev). Furthermore, the transformer, preceding the filter, is also a band-pass device, which bandwidth of 600 MHz results in attenuation of high frequency components (leakage, sum frequency and other mixing products).

When using low-power active mixer, the IF signal has to be amplified to fully drive the ADC. Moreover, requirements specified that new downconverter has to be compatible with the old downconverter board, in which the IF output is connected to the ADC with s coaxial cable. Thus, the new downconverter needs to be able to drive a long coaxial cable and provide enough gain to compensate its attenuation. Therefore, the multichannel downconverter, needed an extra amplifier.

Three solutions were considered for an IF amplifier: monolithic RF amplifier, custom made circuit, and operational amplifier. First solution (e.g. ERA series from Mini-Circuits) is small, requires minimal number of additional components and is cheap. On the other hand, the bandwidth is wide, what requires additional filter to reduce broadband noise. Next, in the active DWC, which has conversion gain, the required amplification is small (especially when the step-up transformer is used for voltage gain), while such gain blocks typically offer gain higher than 10 dB. Furthermore, the gain of such amplifier is not adjustable (although there are different models but this leads to gain stability problems), what limits the modification possibilities.

Second type of amplifier could be custom made circuit. Such solution can be easily modified and its parameters adjusted to meet the specific requirements of the downconverter. However, against such project spoke the cursory nature of the prototype, size of such solution, limited time, cost, and mostly doubt if such circuit can compete with leading company products in the low-noise and low distortion field.

Last option was an operational amplifier (OA). Such solution offers a variety of modifications with small number of additional components needed thus it is small and a low

cost solution. Unfortunately, an overview of the OA market showed that high linearity amplifier can be only found in high speed circuits. For the frequency of interest of maximum 54 MHz amplifiers fulfilling linearity requirements have bandwidth at least ten times wider.

The LMH6702 current feedback amplifier from National Semiconductor was selected, because of low noise (1.8 $nV/\sqrt{Hz}$) and high linearity (–60 dBc). The bandwidth is high (1.7 GHz) but this amplifier features a standard OA footprint[3], what provides an opportunity of exchanging it in case of any problems.

The amplification of the IF signal is performed by two devices: already described in the prototype section step-up transformer, and operational amplifier. The transformer changes the impedance from 50 Ω at the LC filter output to 400 Ω thus increasing the voltage.

The amplifier was used in the non-inverting configuration due to its high input impedance, what resulted in simple input matching network, which is a shunt 400 Ω resistor. The voltage gain was set to +2 using the feedback and gain resistors. Unfortunately, current feedback amplifiers, unlike the voltage feedback amplifiers, are designed for an exactly specified value of the feedback resistor. For LMH6702 this value is equal to 237 Ω (and cannot be decreased without influencing the stability and linearity), what yields about 2.1 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, and from the noise point of view it is dominant noise source compared to 1.8 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ of an amplifier. Using SPICE simulations the RMS noise, introduced by the amplifying stage, has been calculated and resulted in approximately 76 $\mu\mathrm{V_{RMS}}$ in the ADC bandwidth, what is close to the limit of 80 dB SNR.

The role of the output stage is to match the amplifier output to the 50 Ω transmission line and filter out amplifier's harmonics. Basing on the LMH6702 datasheet the output of the amplifier was separated with a 12 Ω series resistor, which act as a buffer, reducing the reactive influence of the following filtering structure. After the filters, matching is realized with series 40 Ω resistor, which gives, with the buffering resistor, impedance of about 50 Ω, while the the output resistance of the operational amplifier is negligible.

The filtering after the OA is done using two elements: high value series capacitor for DC blocking and narrowband (125 MHz) 1:1 transformer (TTWB1010 from Coilcraft). The bandwidth of the LMH6702 amplifier is wide what may lead to the stability problems [26]. The use of the transformer, instead of a simple low-pass RC structure, is safer since the oscillations tend to appear with capacitive loads [26, 11].

After the output network, the IF signal is transmitted through 50 Ω line to the

[3]Unlike the new family of high speed OAs from Analog Devices.

small low-pass filter (LFCN-80 from Mini-Circuits, not visible in Fig.4.9) and then to the IF connector. This filter is placed for experimental purposes or one can say "just in case", it features good high frequency rejection providing good isolation from high order harmonics from operational amplifier or leakage from mixer which could come across stray capacitance between transformer windings. This is achieved at expense of 0.6 dB insertion loss and 1210 package.

The picture of complete board is depicted in Fig. 4.10.

The multichannel downconverter was designed basing on the experience gained on the prototype boards and the experimental results of its measurements are depicted in the following chapter.

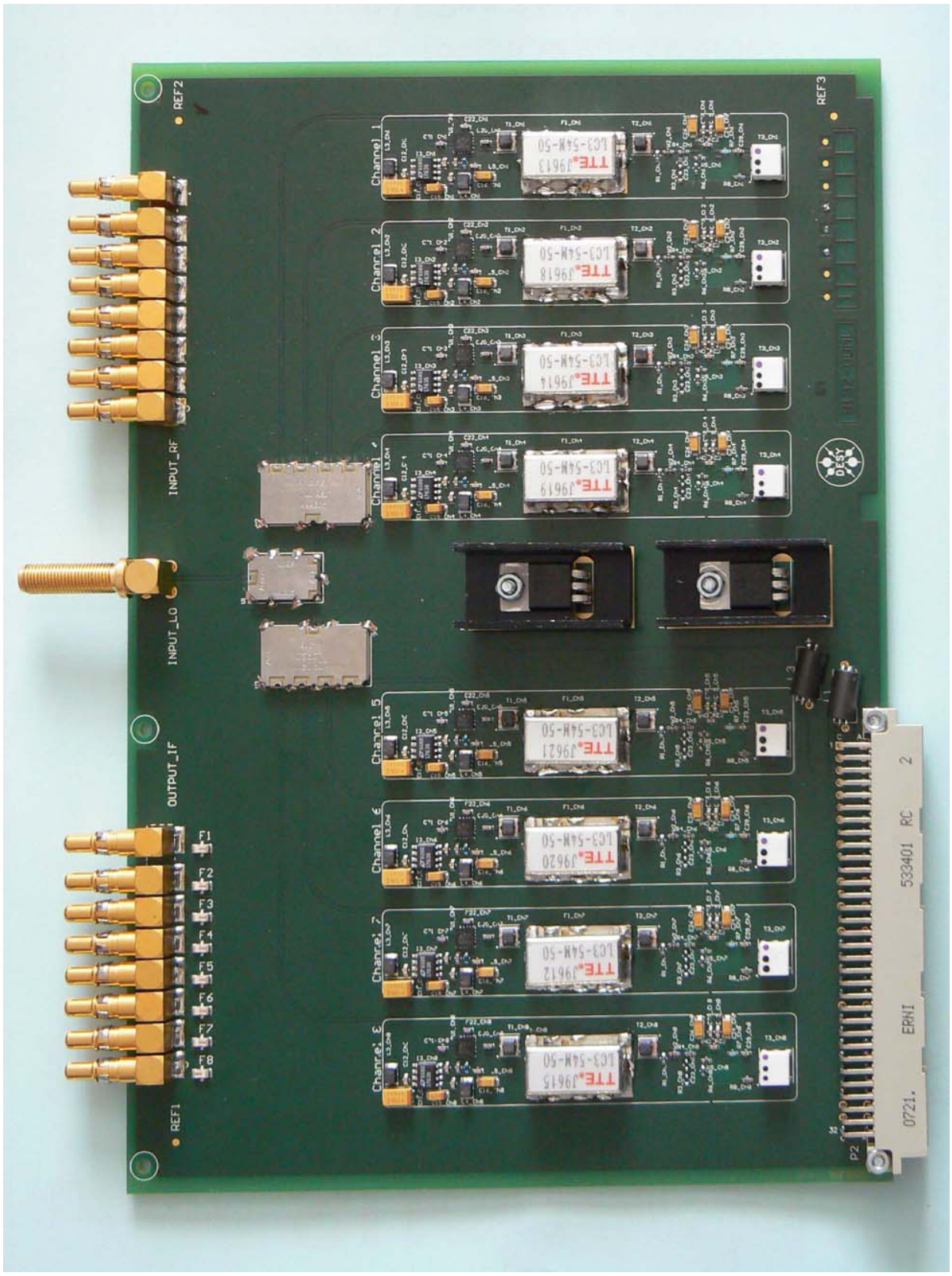

Figure 4.10: Multichannel VME downconverter board.

Chapter 5

Experimental results

The multichannel downconverter, described in the previous section, has been tested and this chapter shows the results.

First, the DWC parameters: linearity and crosstalk are described. Next, the amplitude and phase stability and finally, the measurements of the beam energy, performed in FLASH. At first, downconverter linearity and crosstalk between channels were tested. Then, final tests of the field stability were performed in the FLASH facility and relied on the observation of the beam energy.

All test results were obtained for IF frequency 54 MHz (f_{LO} = 1354 MHz), the LO input power of 7 dBm (-3 dBm at mixer port), and with band-pass filters, unless otherwise specified.

5.1 Linearity

The linearity was tested by checking harmonic distortions and IP_3 with two-tone test [27]. Harmonic content in the output signal of DWC was measured by changing the RF input power, using the step attenuator, to the maximum at +10 dBm. Fig 5.1 depicts the IF output power of fundamental (h1), second (h2) and third harmonic (h3). Harmonic distortion, that is the distance between fundamental and harmonic, is depicted in Fig. 5.2. In the regular operating range (apporx. 0 dBm RF) the downconverter linearity is limited by second harmonic, which is 60 dB lower than the fundamental.

Because of the bandwidth of the band-pass filter (5.4 MHz), the two-tone test is most suitable for DWC nonlinearity description. The IP_3 was measured in the set-up shown in Fig. 5.3, where two generators provide two sine signals which are a little bit spaced in frequency and their sum is fed to the input of the Device-Under-Test (DUT). The input

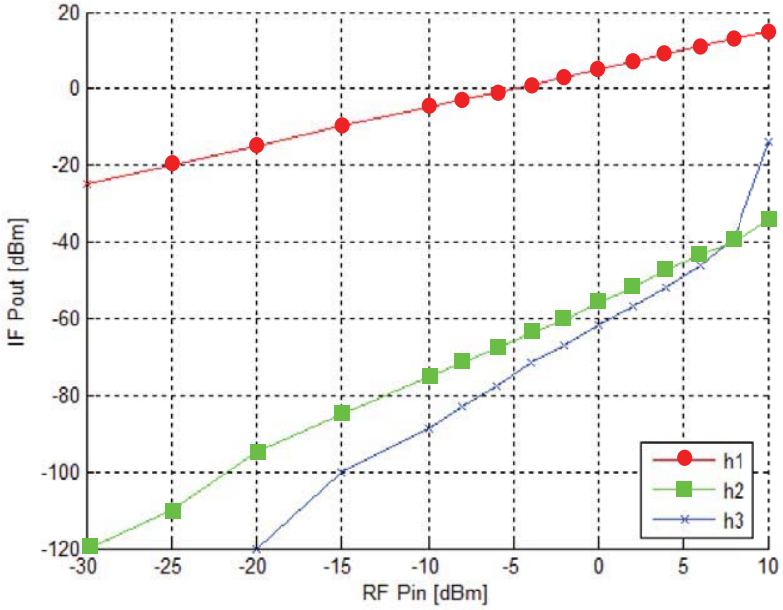

Figure 5.1: Measured output versus input power for the multichannel DWC.

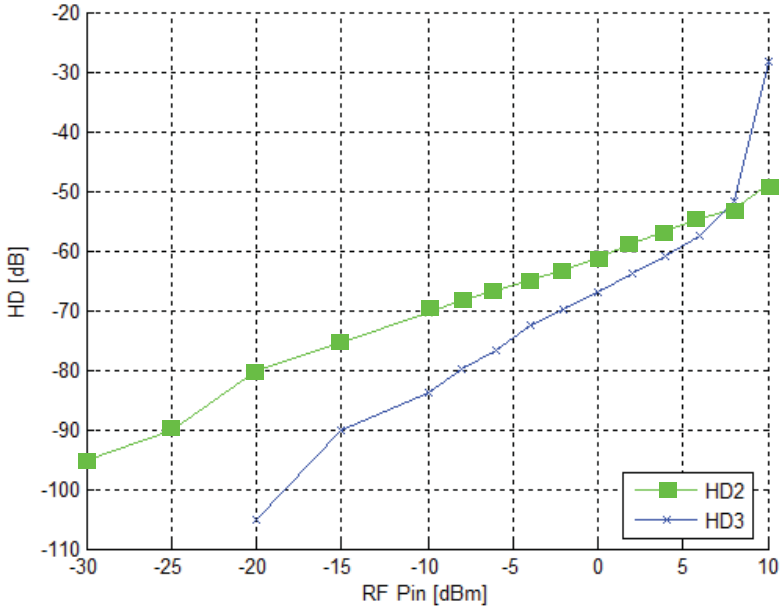

Figure 5.2: Harmonic distortion versus input power for the multichannel DWC.

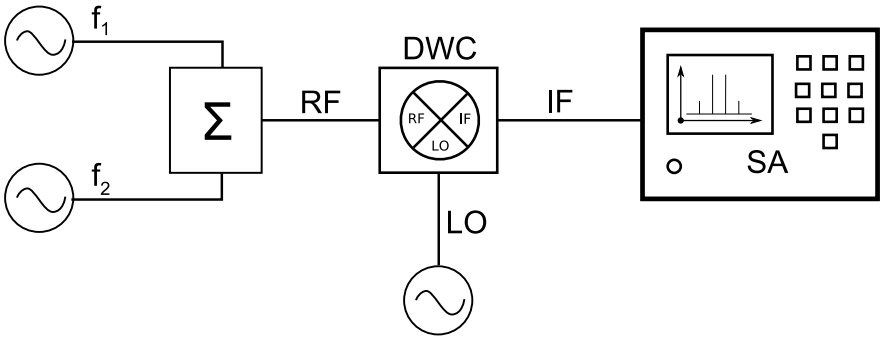

Figure 5.3: Measurement set up for two-tone test.

frequencies were centered around 1.3 GHz with 200 kHz spacing and the input power was set to -11 dBm. To prevent the mutual influence of the generators, additional ferrite isolators (not shown) were used. The IP_3 point, referred to the input or output, was calculated using the following formula [27]:

$$IP3_{\mathrm{IN/OUT}} = \frac{D}{2} + P_{\mathrm{IN/OUT}} \tag{5.1}$$

where P represents the signal power in dBm and D is the distance in dB between the fundamental and intermodulation in the output signal.

The measurement resulted in D=70.4 dB, what yields $IP3_{\mathrm{in}} = 24.2$ dBm. Since the IP_3 of the downconverter is close to the mixer IP_3, given by the manufacturer [20], this means that the output amplifier has negligible contribution.

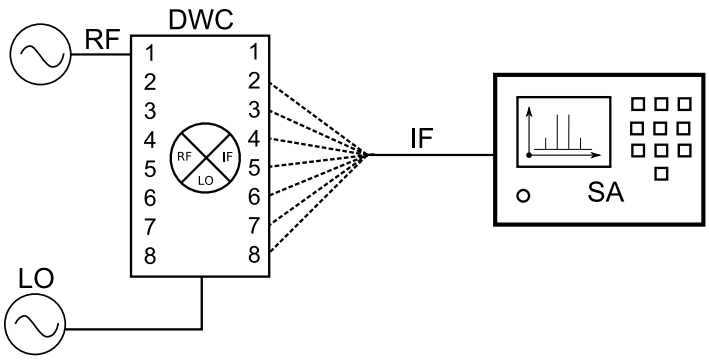

Figure 5.4: Crosstalk measurement set-up.

5.2 Crosstalk

The crosstalk is defined as the amount of the signal, which fed to one channel, is observed in any other and it was measured using set-up from Fig. 5.4. The RF input of one channel of the downconverter was fed with the 1.3 GHz, -5 dBm signal while all other channels were observed for the IF. The crosstalk, from 2nd channel to all others, ranges from 67.1 dB to 70.4 dB. The RF leakage, defined as the power of the 1.3 GHz signal on the IF port of the active channel, was measure66.8 dB.

The results of crosstalk measurement are comparable with those obtained for old DWC. This seems to be caused by similar design of the LO distribution, in which the power divider is used. Any RF signal leaking to the LO port of the mixer, can reach, through the divider, the LO port of another channel. The simplest solution to reduce the crosstalk it to increase the LO power with simultaneous use of the attenuators between the divider and mixer LO port.

5.3 Amplitude and phase instability

The amplitude and phase instability measures as an integral of the appropriate spectral density (see Chapter 2), are hard to apply in practice. Therefore, another definition of instability needs to be introduced. Also, the signal LO generation set-up, for high IF DWC measurements, will be described here.

Amplitude and phase instability can be evaluated statistically by observing the fluctuations of the signal at the detector output. When high precision noise measurements are performed it is crucial to distinguish between the DUT noise and the noise coming from the measurement devices. In case of downconverter measurements, it means that the noise of the RF and LO signal generators must be excluded from the observed

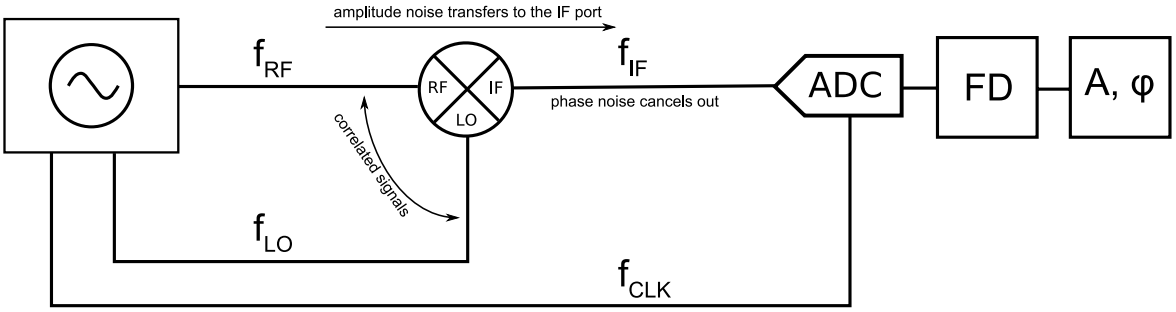

Figure 5.5: Idea of the amplitude and phase instability characterization.

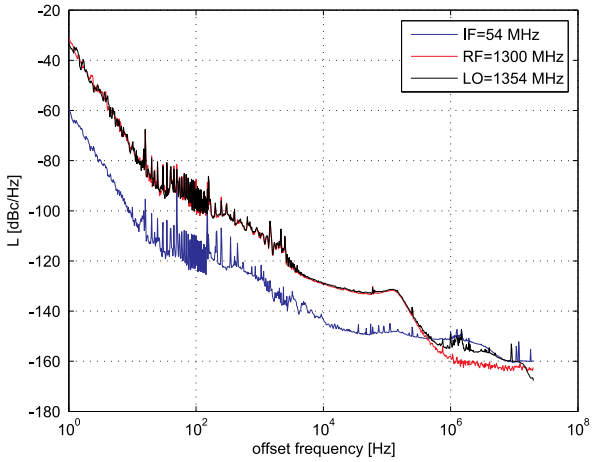

Figure 5.6: Phase noise of RF, LO and IF signals.

fluctuations on the IF port.

The solution can be the idea (proposed by F. Ludwig), depicted in Fig. 5.5, where both DWC input signals are strongly correlated. Due to the mixer properties (2.16), the phase noise of the IF signal should be zero. Any phase noise observed at the DWC output, is the additional noise from the downconverter. However, it is not possible to obtain two fully correlated signals, which differ in frequency. Therefore, the IF port phase noise always contains some amount of the signal generator noise. Another drawback of this concept relates to the amplitude noise, which comes to the IF port from the RF input (2.19). Therefore, to measure proper value of added amplitude noise, a generator featuring low amplitude noise must be used (experiments in this thesis used ultra-low noise Dielectric Resonator Oscillator and the Master Oscillator).

The proof of principle described above, is depicted in Fig. 5.6, the phase noise of three signals was measured: RF (red), LO (black), and IF (blue). The measurement was performed in FLASH, using the MO as the signal generator and the LO generation set-up, which is described in the following paragraphs (Fig. 5.7).

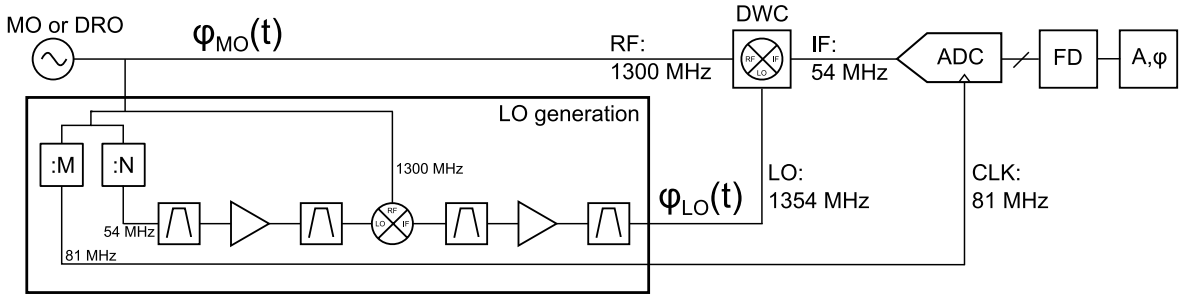

Figure 5.7: Amplitude and phase instability measurement set-up.

The more detailed block diagram of the amplitude and phase instability measurement set-up is depicted in Fig. 5.7. This set-up generates three correlated signals, two for downconverter (RF and LO) and one for the ADC (CLK). Beside the problem of residual phase noise, coming from different frequencies of RF and LO signals, in such set-up the additional noise comes from the LO generation itself due to the use of such sub-components as frequency divider, mixer and amplifiers. Some noise sources can be neglected, like the amplitude noise, some can not, like mixer 1/f noise. However, the influence of the additional noise on the beam stability has not been fully investigated yet, although it was proven experimentally that in this set-up better LO and RF noise cancellation occurs than with two synchronized signal generators [7].

The amount of the noise, observed at the IF output, called here a residual error and can be estimated as follows. Let $\varphi_{MO}(t)$ and $\varphi_{LO}(t)$ represent phase noise of the source and generated LO signal respectively. The object of interest is the residual phase noise defined as the difference between this two values, which, in the ideal case, would be zero. According to [8], the $\varphi_{LO}(t)$ can be described as:

$$\varphi_{LO}(t) = \frac{\varphi_{MO}(t)}{N} + \varphi_N(t) + \varphi_{A1}(t) + \varphi_{\otimes}(t) + \varphi_{MO}(t) + \varphi_{A2}(t), \tag{5.2}$$

where $\varphi_N(t)$ is the additional noise from frequency divider, $\varphi_{A1}(t)$ from the first internal amplifier, $\varphi_{\otimes}(t)$ from the mixer and $\varphi_{A2}(t)$ from the second internal amplifier. Now the residual jitter can be expressed as:

$$\begin{aligned} \varphi_{RES}(t) &= \varphi_{LO}(t) - \varphi_{MO}(t) \\ &= \frac{\varphi_{MO}(t)}{N} + \varphi_N(t) + \varphi_{A1}(t) + \varphi_{\otimes}(t) + \varphi_{MO}(t) + \varphi_{A2}(t) - \varphi_{MO}(t), \end{aligned} \tag{5.3}$$

what can be simplified, by neglecting the amplifiers', mixer and divider noise contribution, to the following formula:

$$\varphi_{RES}(t) = \frac{\varphi_{MO}(t)}{N}. \tag{5.4}$$

Transformation of the equation above to the spectral density domain yields:

$$S_{\varphi_{RES}}(f) = \left(\frac{f_{IF}}{f_{RF}}\right)^2 S_{\varphi_{MO}}(f). \tag{5.5}$$

It is now clearly visible that this residual phase noise contribution can be minimized by se;ecting lower IF frequencies. This is yet another limitation, after ADC performance degradation, which speaks for lower intermediate frequency.

The amplitude and phase instability measurements over time were performed in FLASH to assure that the test conditions are the same as for regular operation. The IF signal from the DWC was sampled by 14 bit ADCs of SIMCON-DSP board [28]. Next, the appropriate IQ detection algorithm calculated the in-phase and quadrature components of the input signal. Then, IQ values were converted to amplitude and phase representation. Relative RMS values were calculated for amplitude $\frac{\Delta A}{A}$ and phase $\Delta\varphi$.

Depending on the period when amplitude/phase is measured we can talk about bunch-to-bunch, pulse-to-pulse instability and short and long term drifts. Bunch spacing in FLASH is $1\mu s$, with maximum flattop time of $800\mu s$, so the stability measured up to 1 ms is called bunch-to-bunch. Repetition rate of FLASH ranges from 1 to 10 Hz so pulse-to-pulse stability is measured in the range of seconds. Longer measurements, above 1 minute, are called drift measurements since slow changes due to temperature variations become visible.

Observations of the amplitude and phase fluctuations over 800 μs are shown in Fig. 5.8, with two colors, each representing different averaging factors. The blue trace stands for one IQ value calculated from 3 raw data samples, which is the minimal value for the IQ detection algorithm for $f_{IF} = 54\ MHz$ and $f_s = 81\ MHz$. Because IQ detection algorithm acts like a digital low-pass filter [7], this corresponds to the bandwidth of $f_s/3 = 27\ MHz$. The red plot was made with 81 raw samples for one IQ value so the effective bandwidth is 1 MHz, what corresponds to the 1 MHz detector bandwidth of the old system. The results of 10 and 60 min. measurements are shown in Fig 5.9 and Fig. 5.10respectively, both for 1 MHz bandwidth. [29]

Time	Bandwidth [MHz]	Amplitude	Phase
800 μs	27	9.34e-4	0.0654
800 μs	1	1.50e-4	0.0092
10 min.	1	1.63e-4	0.0147
60 min.	1	1.81e-4	0.0147

Table 5.1: Results of the amplitude and phase instability measurements.

Table 5.1 summarizes the instability measurements. It gives the RMS results pf the amplitude and phase fluctuations and in case of 60 min drift, it was calculated after linear slope subtraction (Fig. 5.11).

Although the measurements were performed for single channel, due to the properties of the vector-sum system the actual beam energy instability will be $\sqrt{8}$ times smaller thus the 10^{-4} amplitude requirement is fulfilled. Unfortunately, the phase stability is worse, for reason unknown yet. It is supposed that this is a result of additional noise from the LO generation set-up and 1/f noise of the DWC but this problems must be still investigated. Because better LO generation is not known and counteracting flicker noise is difficult, the whole 'IF sampling' concept can be jeopardized.

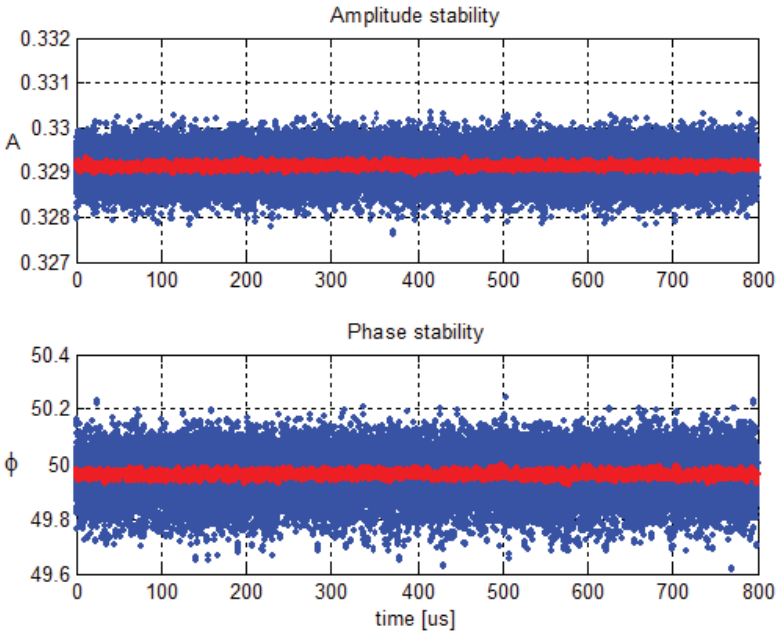

Figure 5.8: Amplitude and phase fluctuations over 800 μs (bunch-to-bunch range). Blue: 27 MHz bandwidth, red: 1 MHz bandwidth.

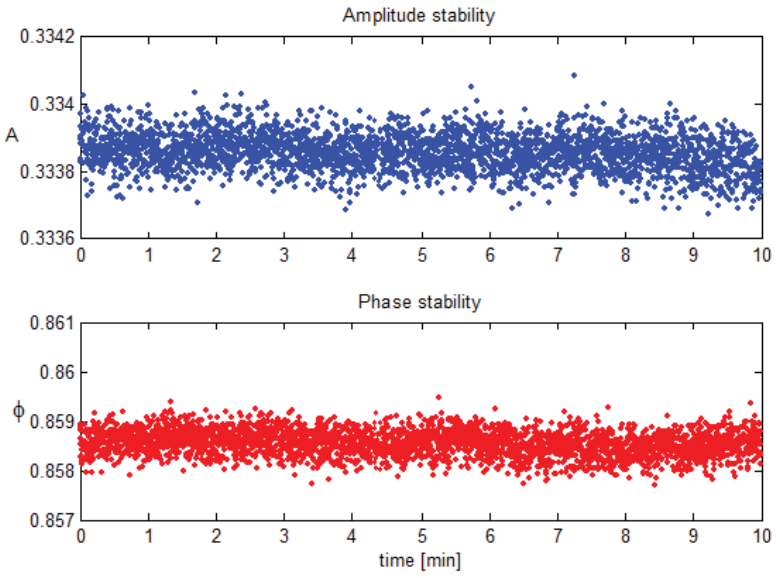

Figure 5.9: Amplitude and phase fluctuations over 10 minutes (pulse-to-pulse range).

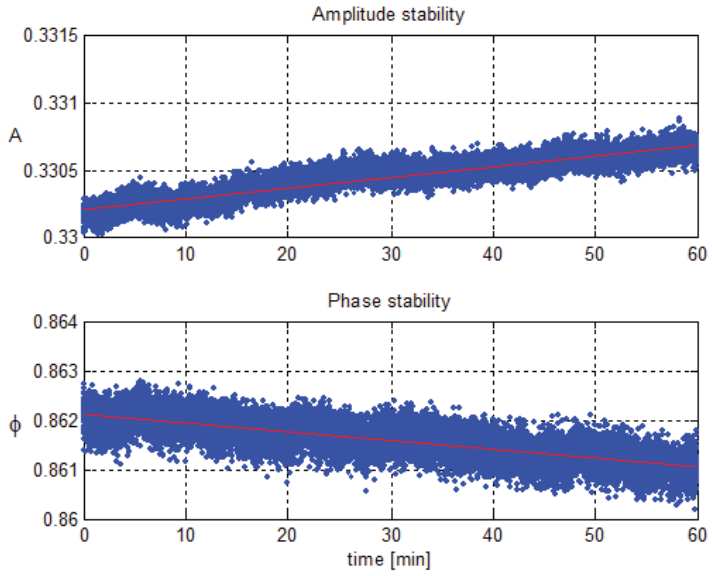

Figure 5.10: Amplitude and phase drift over 60 minutes (drift range).

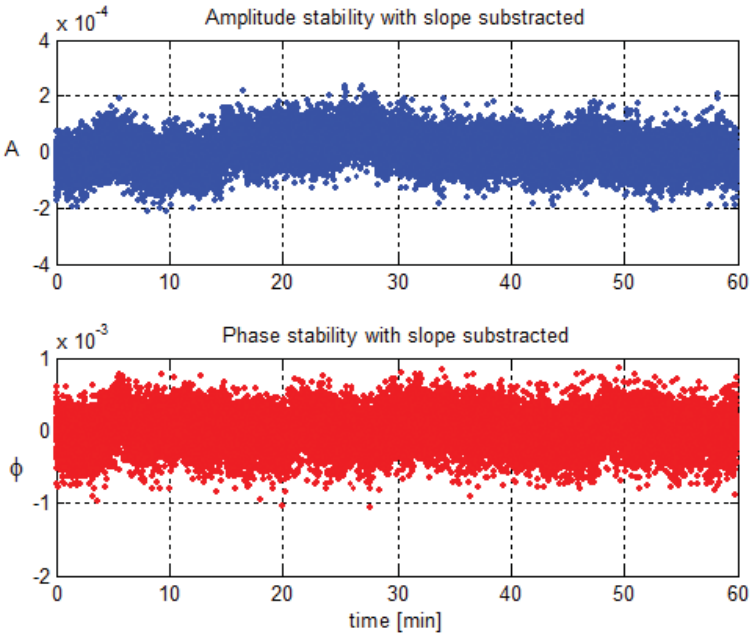

Figure 5.11: Amplitude and phase drift over 60 minutes with subtracted slope.

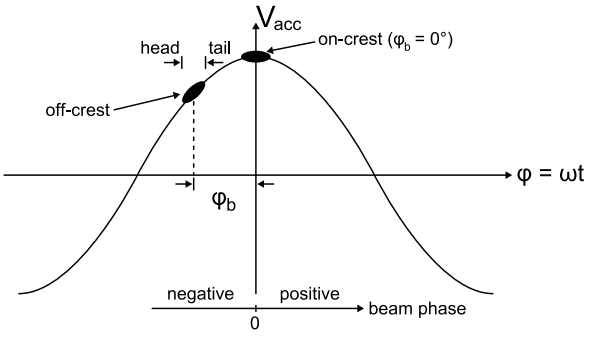

Figure 5.12: Beam phase and corresponding accelerating voltage.

5.4 Beam energy characterization

In the previous section the characterization of stability, for single DWC channel, was described. This section shows the results of beam energy fluctuations, during regular operation, using all eight channels. The beam energy instability was evaluated in FLASH during the test period in September 2007. The experiment was performed using the camera, which measures the intensity of the synchrotron radiation.

The beam is injected into the cavity with respect to the accelerating field, as depicted in Fig. 5.12 [12]. The position of the beam versus the maximum of the electric field is denoted as φ_b. If the beam is injected when the field reaches its maximum we say about on-crest operation ($\varphi_b = 0$). In such conditions, the energy gain of the beam is highest and should not be sensitive to the phase noise of the control system thus only the amplitude noise may influence the stability. The off-crest operation ($\varphi_b \neq 0$) allows shaping of the beam energy profile but in such case the beam energy is also sensitive to phase noise.

The relative beam energy spread $\frac{\Delta_E}{E}$ is described by the following equation [12]:

$$\left(\frac{\Delta E}{E}\right)^2 \cos^2\varphi_b = \frac{1}{2}(1+\cos 2\varphi_b)\left(\frac{\Delta A}{A}\right)^2 + \frac{1}{2}\left(1-\cos(2\varphi_b)\right)\Delta\varphi^2 + \frac{1}{4}\left(3\cos(2\varphi_b)-1\right)\Delta\varphi^4. \quad (5.6)$$

Fig. 5.13 depicts the results of beam energy measurements, performed for different downconverter types:

- Designed multichannel active DWC, on- and off-crest (solid green) and for $f_{IF} = 9$ MHz (hollow green)
- Prototype boards with passive DWC (blue)
- Prototype boards with passive DWC with rough VS calibration (hollow blue)

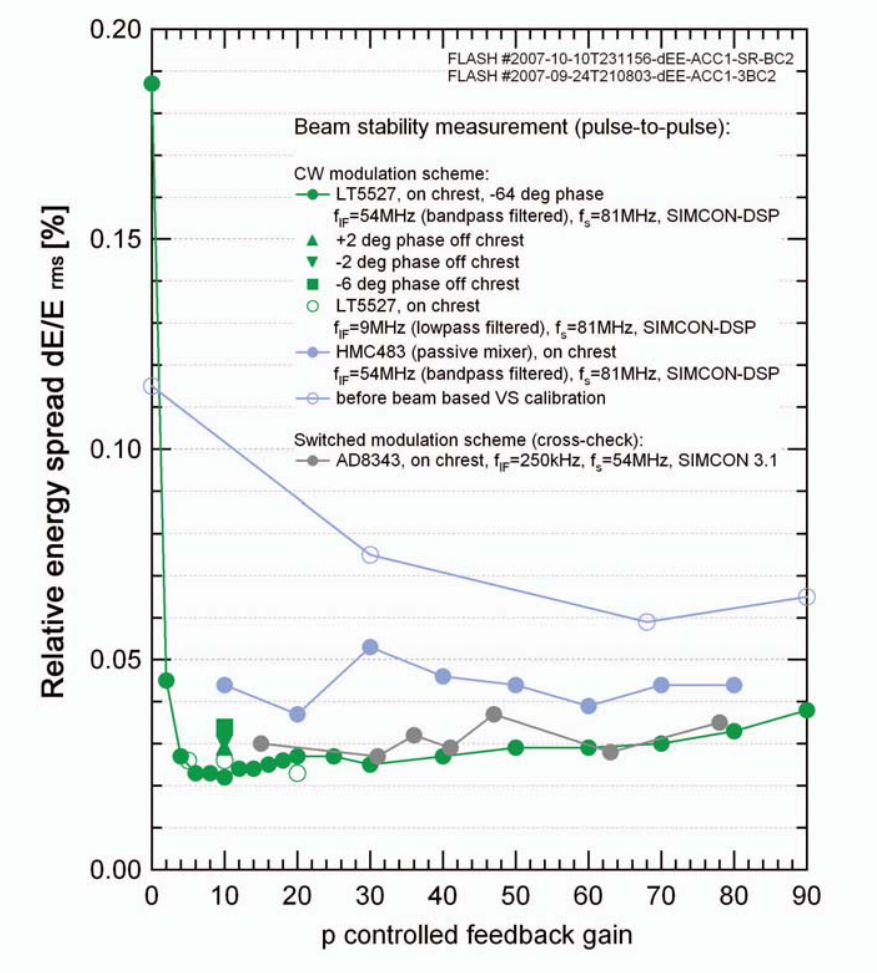

Figure 5.13: Relative beam energy spread versus the loop gain.

- Old system (gray)

The plot shows the relative beam energy spread as the function of the loop gain. One can see that, for multichannel active DWC (green circles), described in Chapter 4, increasing the feedback gain reduces the instability, up to the optimal gain of 10. Further gain increase worsens the stability what origins from increased amount of the detector noise, due to higher loop bandwidth (see Fig. 3.4). However, it was expected that the optimal gain will be few times higher and it is yet unclear what is the reason for this. It is possible that other, undiscovered effect may occur.

Next measurement concerned the on- and off-crest operation, what allowed to distinguish between amplitude and phase noise contribution. For on-crest operation (solid green circles), the stability is better than for off-crest (green triangles and square). This results from different influence of amplitude and phase noise, as described above. How-

ever, the on-crest results are still above the required XFEL limit (0.01%), what means that the amplitude noise was underestimated and further investigation is needed.

The hollow green circles, Fig. 5.13, represent active DWC, operating with $f_{IF} = 9$ MHz. It was expected, that due to the LO generation (described in previous section) and ADC properties, the instability will be smaller but the results showed that the IF change had minor impact. This leads to the conclusion that the ADC performance degradation, when it operates with high IF, is not the limiting factor. More likely the reason lies in the additional noise coming from LO generation, because the set-up is similar both for $f_{LO} = 1354$ MHz and $f_{LO} = 1309$ MHz. Furthermore, the measurements with 9 MHz IF were performed using the downconverter with 54 MHz low-pass filter, thus the harmonics of the signal of interest (18,27,36,ect.) were not attenuated. The similar instability level for 1354 and 1309 MHz may suggest that the nonlinearity issues are overestimated although it must be verified due to low-pass properties of the field detection algorithm.

Next result, plotted in blue in Fig. 5.13, concerns passive downconverter. It was performed by M. Hoffman using prototype DWC boards and ACB2.0 carrier board, described in Chapter 4. It was expected that the passive solution, especially with 16 bit ADCs (compared to 14 bit used in previous measurements), will reach lower instability than its active counterpart. However, almost flat response versus loop gain (solid blue) and lack of characteristic U-shaped curve speaks for measurement error, so the measurement needs to be verified. On the other hand, this measurement showed how vector-sum calibration error can eclipse all other error sources (hollow blue).

As a comparison, the old system was measured during the same measurement shift (gray). The results show that high IF system is just slightly better than the old one but the XFEL requirements are not fulfilled. This leads to the conclusion that further investigation of noise sources in the control system is needed.

Chapter 6

Summary

The goal of this thesis was to design a new downconverter type, which fulfills the requirements foreseen for the new XFEL accelerator. The development has been carried out from concept through prototype boards to multichannel downconverter board and also embraced the experiments in the FLASH facility.

The concept originates from F. Ludwig and M. Hoffmann ideas [7] and was based on mixer-filter-amplifier chain. In such configuration the mixer is responsible for frequency shifting, the filter removes unwanted harmonics while the amplifier adjusts the output signal for optimal range of the following ADC.

To achieve required 10^{-4} stability of amplitude and phase, many factors had to be considered during the design. In the downconverter main contributors to the instability of the IF signal are noise and nonlinearities introduced by the circuit itself thus must be minimized by careful design. However, reducing the influence of these error sources at the same time is difficult because of the design of the electronic components. In practice, high linearity devices usually do not feature low noise and vice versa or would require high amount of input power, making the design impractical in large scale applications like XFEL. Therefore a compromise had to be established. Unfortunately it was unclear how each of these factors affects the beam stability and that is why the design of the prototypes was splitted into two, parallel (because of time constraints) paths.

The prototype boards were designed using passive (M. Hoffmann) and active mixer IC (author). The passive device features low noise while the active one is more linear. Due to required high LO power of the passive solution, the appropriate chip HMC483, containing internal LO amplifier was selected. The active solution based on Gilbert-cell mixer LT5527. Although the concept assumed the usage of the IF amplifier, in the prototype boards, to achieve 'as good as it can get' performance the amplifier was neglected

and the downconverter was integrated with the following ADC in one metal housing, which provided good grounding and shielding. The integration was done using special carrier board (ACB 2.0) instead of the usual SIMCON controller but unfortunately, due to mishap, led to project delay.

The prototype boards served as the base for the development of the multichannel downconverter but at this point it is necessary to say, that the experiments, which based on developed downconverters, were limited in time therefore some areas, which fell behind the schedule were not described (e.g. prototype boards experimental results).

This thesis describes the development of multichannel downconverter, based on the active mixer, while the passive version was developed by an external company and did not meet the time schedule thus was not produced. In the multichannel design additional problems had to be considered, mostly crosstalk, LO signal distribution (compactness) and IF amplification issues. To easily show the performance improvement the designed solution had to be compatible with an old downconverter, thus it had to be able to send the IF signal through long coaxial cable to the controller board. Therefore the IF amplifier had to be included into the design and its performance (noise, linearity) considered. The LMH6702 operational amplifier was selected because it features low noise and high linearity, but this comes with high 1.7 GHz bandwidth. Therefore, to avoid oscillations from such fast amplifier, special care was paid when making the layout, like minimizing stray capacitance or assuring proper ground. However, it was expected that the performance of the multichannel board will be degraded, comparing to the prototype, because of crosstalk, additional noise from IF amplifier and lower bit resolution of the old controller (14-bit) compared to 16-bit ADC on the ACB 2.0 carrier board.

After manufacturing, the multichannel DWC was tested in the laboratory environment, for linearity, crosstalk and amplitude and phase stability. Special LO generation set-up was proposed (by F. Ludwig) to eliminate the influence of the generator noise on the IF signal. Next step was performed during test period in FLASH facility, when the beam energy spread was measured, providing the ultimate quality factor of the new downconverter.

The analysis of the experimental results showed that in laboratory conditions the stability requirements are only partially fulfilled and the phase instability is few times higher than expected but the reason is still unknown. One explanation can lie in the LO generation set-up, which adds additional noise to the system but this still must be investigated through theory development and simulations.

This thesis serves as the base for future developments. It answered a few problems and

also set new questions. The measurements performed in FLASH changed the knowledge about two noise components: 1/f noise and high frequency noise. For the long time, it was assumed that the high frequency noise is the major contributor to the control system. The background of this assumption was that the HF noise is clearly visible in the diagnostic system. The measurements with the new downconverter shown that the HF noise is mostly a 'display problem' because the narrow-band cavity filters it out though it is not transported onto the beam. Still, HF noise is responsible for the signal-to-noise ratio of the sampled IF signal and it influences the field measurement.

Next, the results showed that the flicker noise was underestimated. The flicker noise is the source of the slow fluctuations in the energy of the synchrotron radiation. These variations are in the pulse-to-pulse range and are main contributor when analyzing beam energy stability. The exact origin of the flicker noise, in the control system, is not known yet. The measurements, carried out in the accelerator, showed that the most probable are the LO generation set-up and the input stage of the downconverter. If the influence of the LO generation set-up will be confirmed, further developments if the high IF scheme can be jeopardized.

Another important noise contributor is the analog-to-digital converter. Although the ADC is not technically a part of the downconverter, it plays a vital role as the part of the cavity field detector. The simulations performed during the downconverter design process (M. Hoffmann) showed that the ADC is the biggest noise contributor in the detector chain. Therefore, further developments of the detector, will use ADCs with higher bit number.

This thesis sets the goals for the future development. To achieve 10^{-4} stability, in amplitude and phase, the described design can be used. It provides satisfactory performance with low input power thus it can be used in the main section of the accelerator new accelerator, where the requirements are lower. For higher performance, needed in the first sections of the machine, some modifications will be needed and probably high power, low 1/f noise passive mixers will be used.

Appendices

Appendix A

Multichannel DWC – PCB

During the design process some difficulties had to be overcome. First thing which was carefully planned was the layerstack. Eight separate layers was foreseen:

1 – LO signal distribution and vast majority of the components

2 – ground plane for LO and RF signals

3 – RF signals distribution

4 – ground plane for RF signals

5 – +5 V power plane

6 – –5 V power plane (acts as ground for the IF signals)

7 – IF signals distribution

8 – rest of the components and ground plane for IF signals.

This kind of "sandwich" structure isolates both RF and IF signals from electromagnetic distortions. To keep costs low the chosen material was FR4. Even though FR4 is not specified for microwave range it was decided to use it since the maximum frequency was only 1.3 GHz, matching was not the bottleneck of the system and the board manufacturer offered impedance control. Unfortunately this solution has disadvantage – calculating the width of 50 Ω line gave result around 5 mil[1] which is not only the current technology limit but also a point where small edge imperfections can strongly influence the impedance of the transmission line. The only solution to this problem was to increase the thickness of each layer. This resulted in increased thickness of the whole board so the edges had to

[1] 1 mil=1/1000"=0.0254 mm

be milled to fit in 1.6 mm VME slot. One exception was made for power planes - the distance between two power planes was decreased to 0.1 mm to increase stray capacitance between those layers.

Second issue was good RF design since 16 microwave signals ($8 \times$RF and $8 \times$LO) were distributed over the DWC board. This was made by careful design of the microstrip and stripline transmission lines, using soft bends, surrounding lines with vias to ground plane, assuring good ground connection around connectors and RF components. Although the "sandwich" structure of the layerstack reduced the crosstalk, care was taken to route the transmission lines in a way that would minimize the intersections.

Next problem was the wide bandwidth of the operational amplifier (1.7 GHz). With such fast amplifier there is a big risk of oscillations unless appropriate steps are taken [26],[11]. Therefore, special attention was paid when making layout around the operational amplifier: copper beneath amplifier was removed from all eight layers to minimize parasitic capacitance; the length of the feedback path from output to the inverting input was minimized by putting amplifier chip on the bottom side of the board; the ground of power supply decoupling capacitors was put away from the signal ground; decoupling capacitors were used not only between positive/negative power supply and ground but also between power planes, what reduces the harmonic distortion [24].

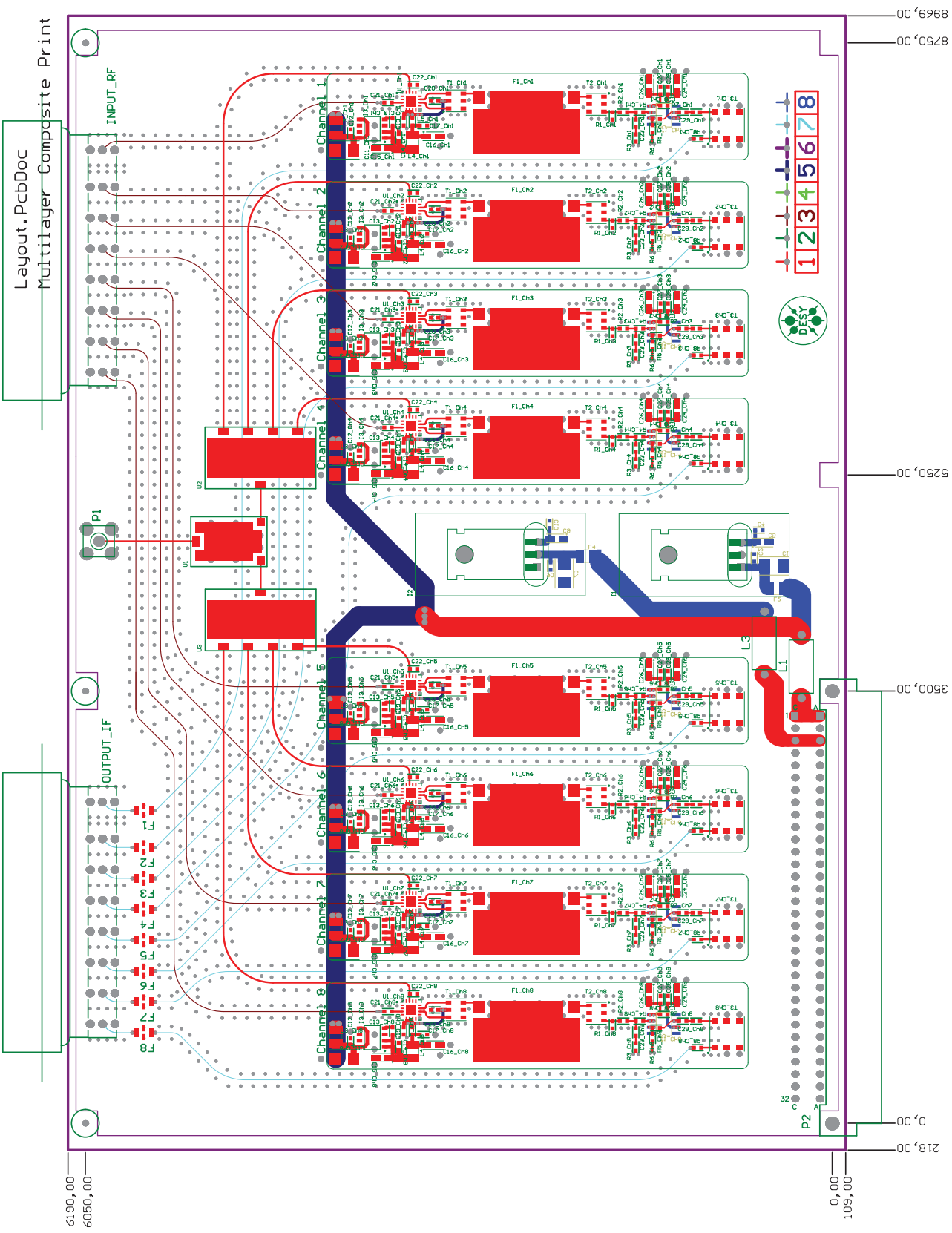

Figure A.1: Layout of the VME downconverter.

The board, depicted in Fig. A.1, contains eight separate channels, so it is capable of mixing eight different signals from eight cavities. In this way, one DWC board can handle the full set of probe signals from one cryomodule. The board's dimensions are specified by VME 6U size C standard (233×160mm). Although DWC operates in EURO crate only power supply pins are used. The board consists of eight layers and the components are mounted on both sides. There are two high frequency FMX connectors for RF input and IF output, each consisting of eight subconnectors. The LO signal is connected to the board through SMA connector and splitted eight-way (2-way splitter followed by two 4-way splitters) and it is distributed on the top layer. The supply voltage (± 15 V), taken from the VME connector, biases ten voltage regulators: eight for mixers and two for operational amplifiers.

The multichannel downconverter, as a prototype board, gives many modification opportunities:

- **IF frequency** – The IF frequency can be easily changed by filter replacement, if carefully considered, a low-pass filter can be used allowing user to make "IF scan" providing information on selection the best intermediate frequency. The filtering section is the one and only one when one wants to change the IF.

- **IF filtering** – The IF filter can be replaced for different frequency but also it can be removed and its pads can be shorted. This will allow user to experiment with four component placeholders which are meant to serve as simple RC filtering structure. Simple low-pass filters in surface mount technology can be easily implemented.

- **Output filtering** – Output filtering structure can also be changed. Default configuration assumes filtering by a narrowband transformer but RC filter is also possible from construction point of view. Furthermore SMD filters, following output stage, can be easily shorted or exchanged.

- **OA replacement** – The operational amplifier used in the design has standard footprint (contrary to the new footprint used in Analog Devices high speed amplifiers), so in case of e.g. stability problems or when better device is available, it can be easily exchanged.

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